

# M3818x Group

## SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

### DESCRIPTION

The M3818x group is made up of 8-bit microcomputers based on the MELPS 740 core.

The M3816x group is designed mainly for VCR timer/function control, and include six 8-bit timers, a fluorescent display automatic display circuit, a PWM function, and an 8-channel A-D converter.

The various microcomputers in the M3818x group include variations of internal memory size and packaging. For details, see the section on part numbering.

### FEATURES

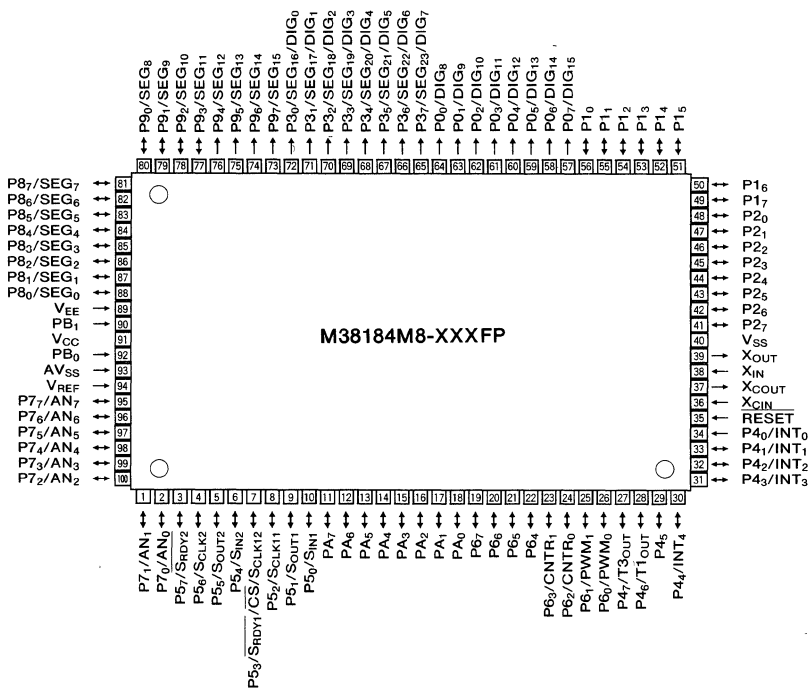
- Basic machine-language instructions ..... 71
- Instruction execution time ..... 0.63μs (shortest instruction at 6.3MHz oscillation frequency)
- Memory size
  - ROM ..... 4K to 40K bytes
  - RAM ..... 192 to 1024 bytes
- Programmable input/output ports ..... 67
- High-breakdown-voltage output ports ..... 32
- Interrupts ..... 18 sources, 15 vectors

- Timers ..... 8-bit×6
- Serial I/O ..... Clock-synchronized 8-bit×2 (Serial I/O1 has an automatic data transfer function)
- PWM output circuit ..... 14-bit×1  
8-bit×1 (also functions as timer 6)
- A-D converter ..... 8-bit×8 channels
- Fluorescent display function
  - Segments ..... 8 to 24
  - Digits ..... 4 to 16
- 2 Clock generation circuit
  - Clock (X<sub>IN</sub>-X<sub>OUT</sub>) ..... Internal feedback amplifier
  - Sub clock (X<sub>CIN</sub>-X<sub>COUT</sub>) ..... Internal amplifier without feedback
- Supply voltage ..... 4.0 to 5.5V
- Low power dissipation
  - In high-speed operation ..... 38mW (at 6.3MHz oscillation frequency)
  - In low-speed operation ..... 300μW (at 32kHz oscillation frequency)
- Operating temperature range ..... -10 to 85°C

### APPLICATIONS

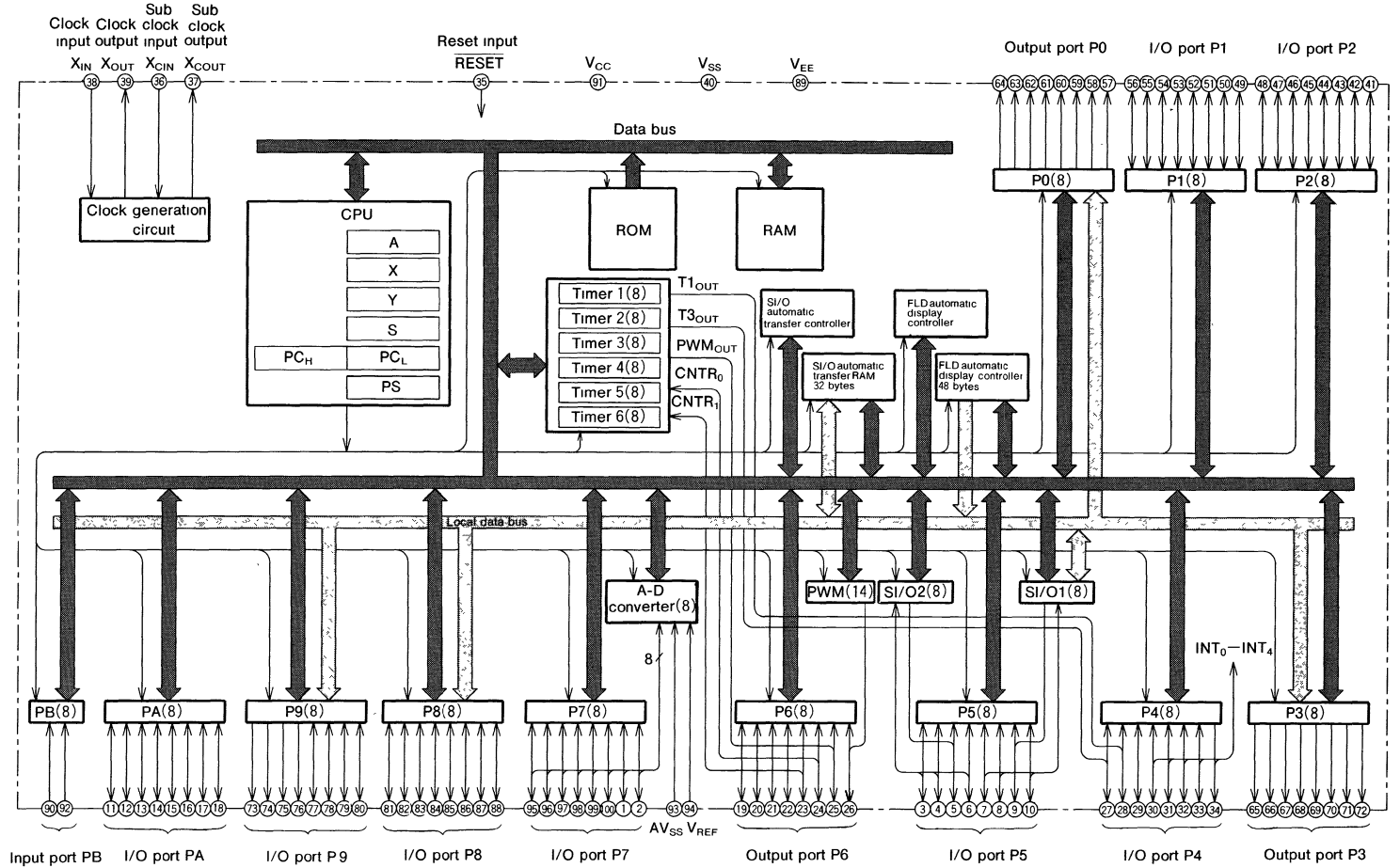
VCRs, microwave ovens, domestic appliances, ECRs, etc.

### PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S  
100-pin plastic molded QFP

# FUNCTIONAL BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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## SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V <sub>CC</sub> , V <sub>SS</sub>	Power supply	Power supply inputs 4.0 to 5.5V to V <sub>CC</sub> , and 0V to V <sub>SS</sub> .	
V <sub>EE</sub>	Pull-down power input	Applies voltage supplied to pull-down resistors of ports P0, P3 and 8	
V <sub>REF</sub>	Analog reference voltage input	Reference voltage input pin for A-D converter	
AV <sub>SS</sub>	Analog power supply	GND input pin for A-D converter. Keep at the same potential as V <sub>SS</sub> .	
RESET	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under high-speed operating conditions. In low-speed operation start mode, internal reset is not released until the X <sub>CIN</sub> -X <sub>COU</sub> T clock has had time to stabilize.	
X <sub>IN</sub>	Clock input	Input and output signals for the internal clock generation circuit. It consists of internal feedback amplifier. Connect a ceramic resonator or quartz crystal between the X <sub>IN</sub> and X <sub>OUT</sub> pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X <sub>IN</sub> pin and leave the X <sub>OUT</sub> pin open. This clock is used as system clock.	
X <sub>OUT</sub>	Clock output		
X <sub>CIN</sub>	Sub clock input	Input and output signals for the internal sub clock generation circuit. It consists of internal amplifier without feedback. Connect a ceramic resonator or quartz crystal and external feedback resistor between the X <sub>CIN</sub> and X <sub>COU</sub> T pins. If an external clock is used, connect the clock source to the X <sub>CIN</sub> pin and leave the X <sub>COU</sub> T pin open. This clock can also be used as the system clock.	
X <sub>COU</sub> T	Sub clock output		
P0 <sub>0</sub> /DIG <sub>8</sub> - P0 <sub>7</sub> /DIG <sub>15</sub>	Output port P0	An 8-bit output port. The output structure is high-breakdown-voltage P-channel open drain with internal pull-down resistors connected between the output and the V <sub>EE</sub> pin. Are "L" at reset.	FLD automatic display pins
P1 <sub>0</sub> -P1 <sub>7</sub>	I/O port P1	An 8-bit CMOS I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. At reset this port is set to input mode. The input levels are CMOS compatible.	
P2 <sub>0</sub> -P2 <sub>7</sub>	I/O port P2	An 8-bit CMOS I/O port with the same function as port P1. The input levels are TTL compatible.	
P3 <sub>0</sub> /SEG <sub>16</sub> / DIG <sub>0</sub> -P3 <sub>7</sub> / SEG <sub>23</sub> /DIG <sub>7</sub>	Output port P3	An 8-bit output port with the same function as port P0.	FLD automatic display pins
P4 <sub>0</sub> /INT <sub>0</sub>	Input port P4 <sub>0</sub>	A 1-bit CMOS input port.	External interrupt input pin
P4 <sub>1</sub> /INT <sub>1</sub> - P4 <sub>4</sub> /INT <sub>4</sub>	I/O port P4	A 7-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels.	External interrupt input pins
P4 <sub>5</sub>			
P4 <sub>6</sub> /T1 <sub>OUT</sub> - P4 <sub>7</sub> /T3 <sub>OUT</sub>			Timer output pin
P5 <sub>0</sub> /S <sub>IN1</sub> , P5 <sub>1</sub> /S <sub>OUT1</sub> , P5 <sub>2</sub> /S <sub>CLK1</sub> , P5 <sub>3</sub> /S <sub>RDY1</sub> / CS/S <sub>CLK12</sub>	I/O port P5	An 8-bit I/O port with the same function as port P1. The output structure of this port is N-channel open drain, and the input levels are CMOS compatible. Keep the input voltage of this port between 0V and V <sub>CC</sub> .	Serial I/O1 I/O pins
P5 <sub>4</sub> /S <sub>IN2</sub> , P5 <sub>5</sub> /S <sub>OUT2</sub> , P5 <sub>6</sub> /S <sub>CLK2</sub> , P5 <sub>7</sub> /S <sub>RDY2</sub>			Serial I/O2 I/O pins

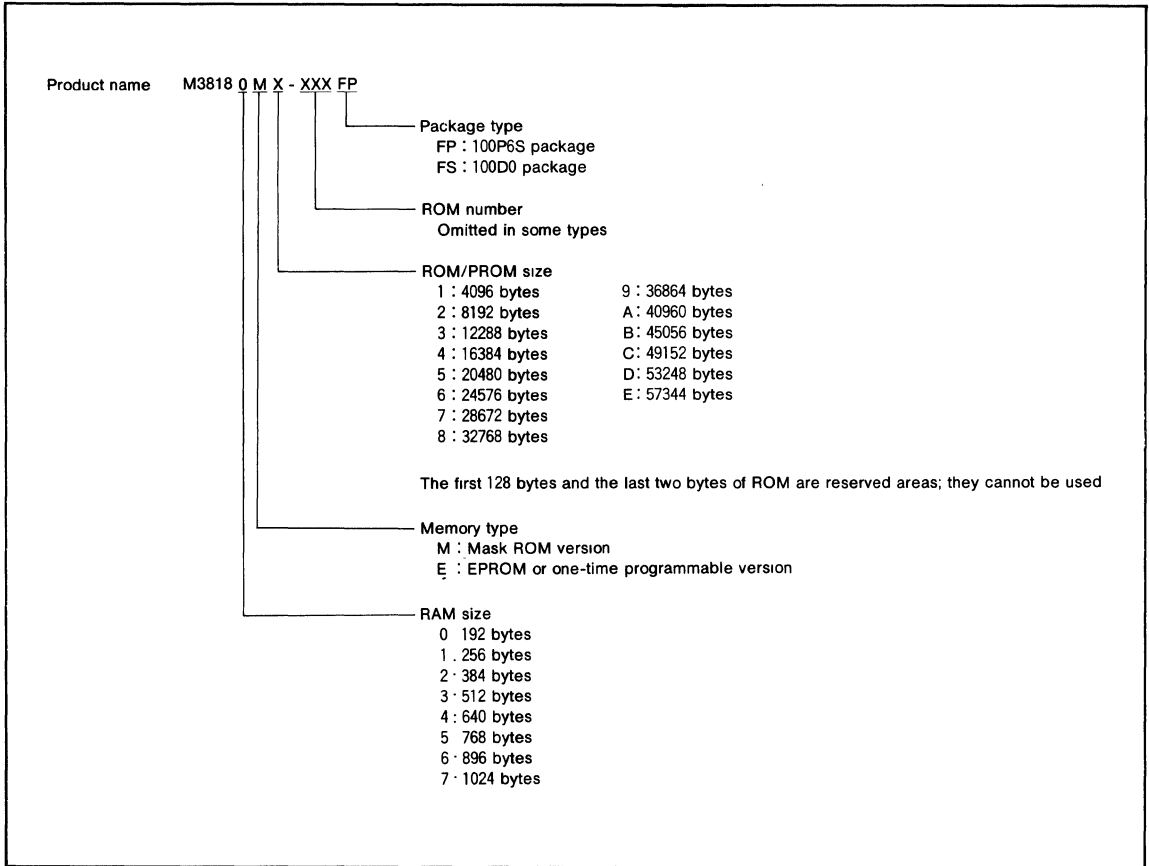
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Function	Alternate Function
P6 <sub>0</sub> /PWM <sub>0</sub>	I/O port P6	An 8-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	14-bit PWM output pin
P6 <sub>1</sub> /PWM <sub>1</sub>			8-bit PWM output pin
P6 <sub>2</sub> /CNTR <sub>0</sub> , P6 <sub>3</sub> /CNTR <sub>1</sub>			Event counter input pins
P6 <sub>4</sub> — P6 <sub>7</sub>			
P7 <sub>0</sub> /AN <sub>0</sub> — P7 <sub>7</sub> /AN <sub>7</sub>	I/O port P7	An 8-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	A-D converter input pins
P8 <sub>0</sub> /SEG <sub>0</sub> — P8 <sub>7</sub> /SEG <sub>7</sub>	I/O port P8	An 8-bit I/O port with the same function as port P1. The output structure of this port is P-channel open drain, and the input levels are CMOS compatible. Please note that this port does not have internal pull-down resistors.	FLD automatic display pins
P9 <sub>0</sub> /SEG <sub>8</sub> — P9 <sub>3</sub> /SEG <sub>11</sub>	I/O port P9	A 4-bit I/O port with the same function as port P1. The output structure of this port is P-channel open drain, and the input levels are CMOS compatible. This port has internal pull-down resistors.	FLD automatic display pins
P9 <sub>4</sub> /SEG <sub>12</sub> — P9 <sub>7</sub> /SEG <sub>15</sub>	Output port P9	A 4-bit output port with the same function as port P0	FLD automatic display pins
PA <sub>0</sub> —PA <sub>7</sub>	I/O port PA	An 8-bit CMOS I/O port with the same function as port P1, with CMOS compatible input levels	
PB <sub>0</sub> , PB <sub>1</sub>	Input port PB	A 2-bit CMOS input port	

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**PART NUMBERING**

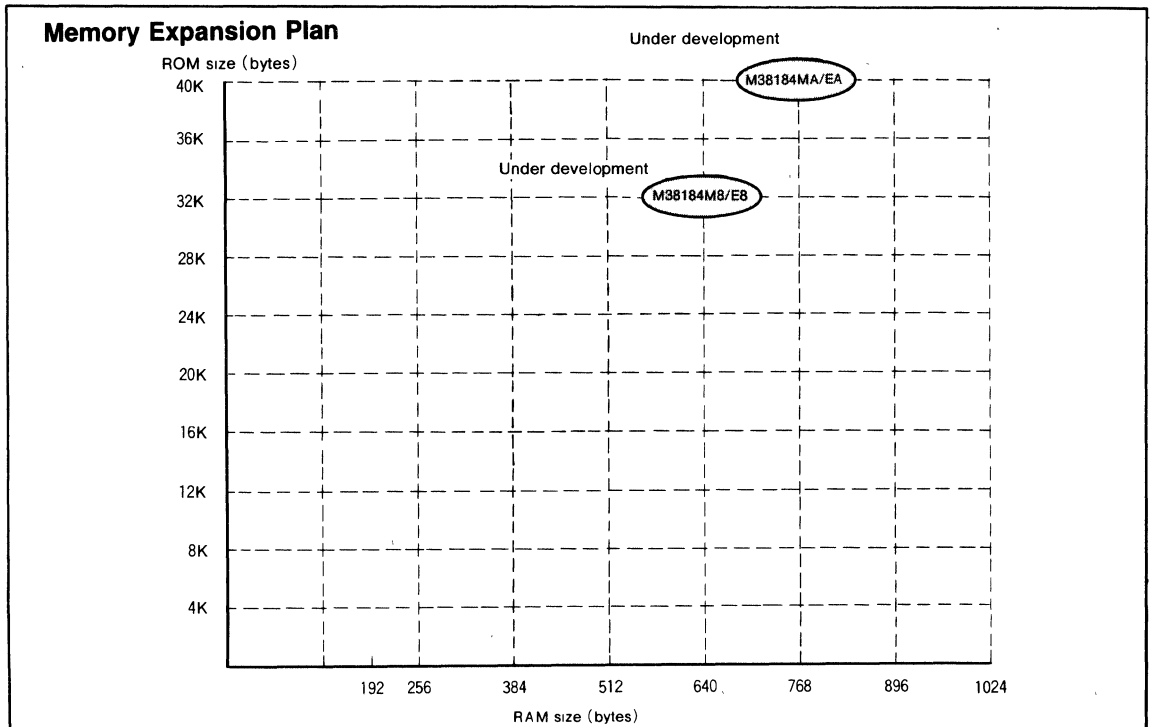


**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**GROUP EXPANSION**

Mitsubishi plans to expand the M3818x group as follows:

- (1) Support for mask ROM, one-time programmable, and EPROM versions
- (2) ROM/PROM size .....32K to 40K bytes  
 RAM size ..... 640 bytes
- (3) Packages  
 100P6S .....Plastic molded QFP  
 100D0 .....Window type ceramic LCC



The development schedule and other details of products under development may be revised without notice

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**FUNCTIONAL DESCRIPTION  
 CENTRAL PROCESSING UNIT (CPU)**

Microcomputers of the M3818x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions, or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:

- The FST and SLW instructions are not available for use.
- The STP, WIT, MUL and DIV instructions can be used.

**CPU MODE REGISTER**

The CPU mode register is allocated to address 003B<sub>16</sub>.

Bits 0 and 1 of this register are processor mode bits and should always be set to "0".

The CPU mode register contains the stack page selection bit.

For details of the X<sub>COU</sub>T drivability selection bit, main clock stop bit, and internal system clock selection bit, see the section on the clock generation circuit.

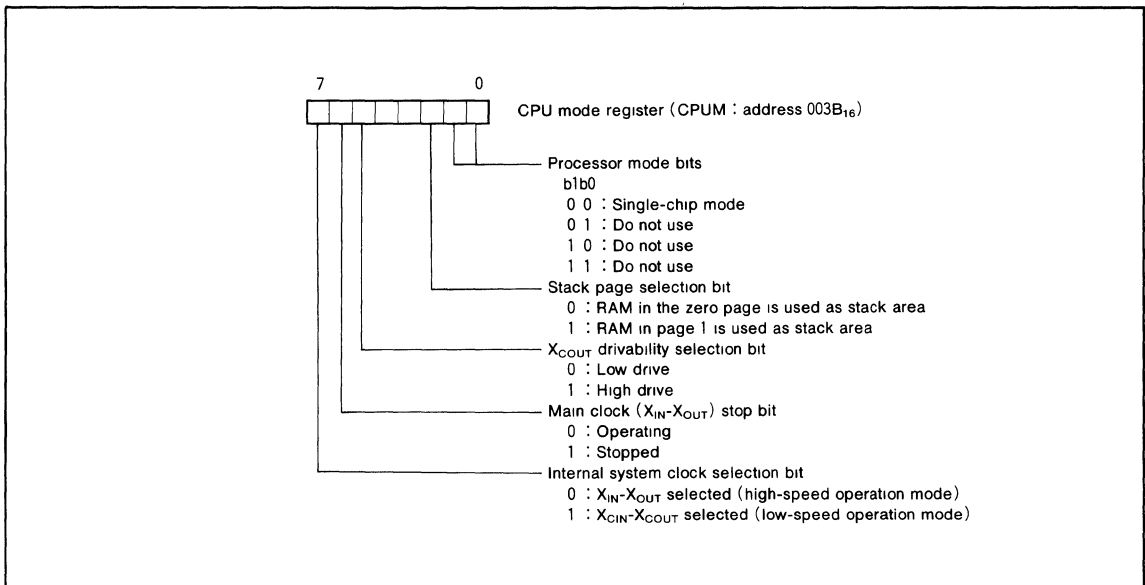


Fig. 1 Structure of CPU mode register

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**MEMORY**

• **Special Function Register (SFR) Area**

The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.

• **RAM**

RAM is used for data storage as well for stack area.

• **ROM**

The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.

• **Interrupt Vector Area**

The interrupt vector area contains reset and interrupt vectors.

• **Zero Page**

The 256 bytes from addresses  $0000_{16}$  to  $00FF_{16}$  are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.

• **Special Page**

The 256 bytes from addresses  $FF00_{16}$  to  $FFFF_{16}$  are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

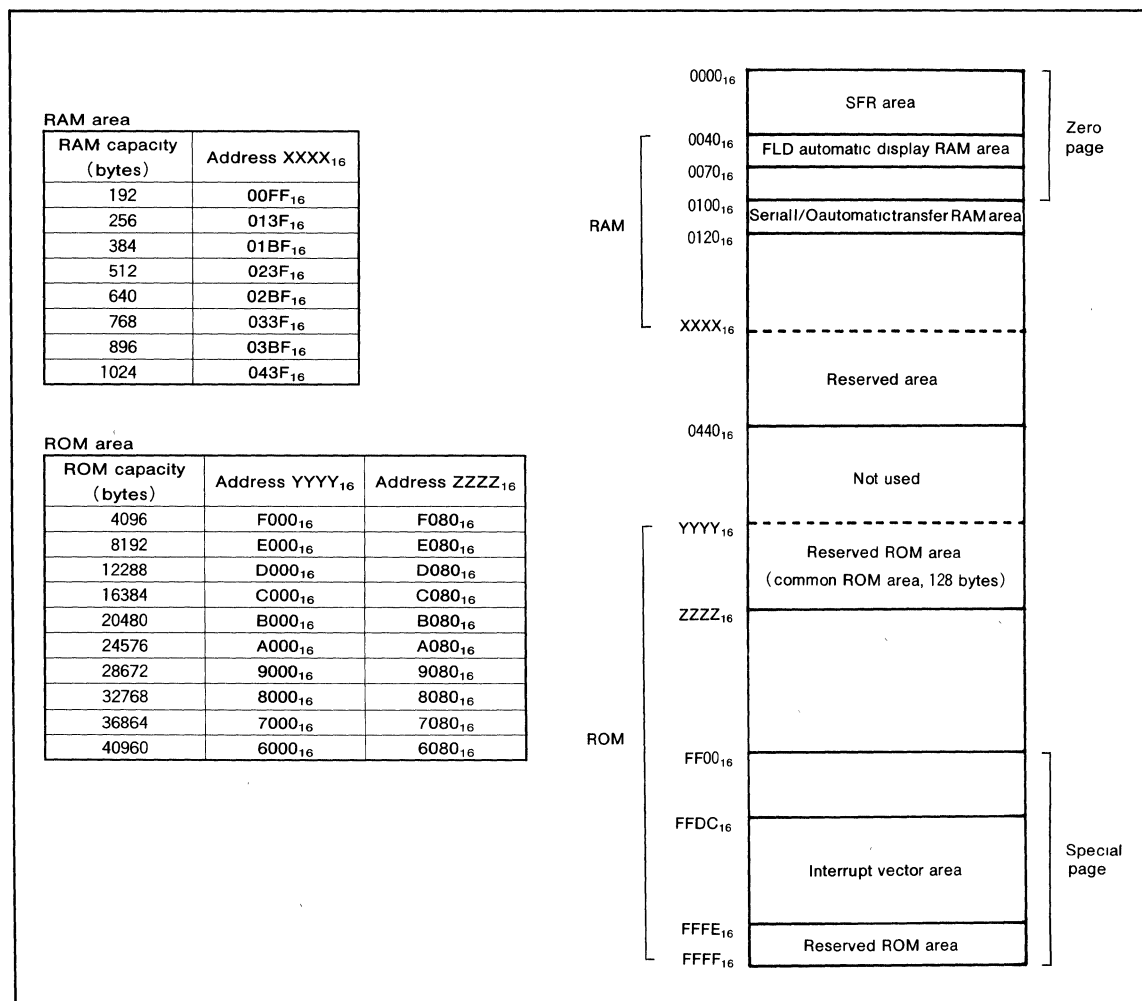


Fig. 2 Memory map diagram



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

0000 <sub>16</sub>	Port P0 (P0)
0001 <sub>16</sub>	
0002 <sub>16</sub>	Port P1 (P1)
0003 <sub>16</sub>	Port P1 direction register (P1D)
0004 <sub>16</sub>	Port P2 (P2)
0005 <sub>16</sub>	Port P2 direction register (P2D)
0006 <sub>16</sub>	Port P3 (P3)
0007 <sub>16</sub>	
0008 <sub>16</sub>	Port P4 (P4)
0009 <sub>16</sub>	Port P4 direction register (P4D)
000A <sub>16</sub>	Port P5 (P5)
000B <sub>16</sub>	Port P5 direction register (P5D)
000C <sub>16</sub>	Port P6 (P6)
000D <sub>16</sub>	Port P6 direction register (P6D)
000E <sub>16</sub>	Port P7 (P7)
000F <sub>16</sub>	Port P7 direction register (P7D)
0010 <sub>16</sub>	Port P8 (P8)
0011 <sub>16</sub>	Port P8 direction register (P8D)
0012 <sub>16</sub>	Port P9 (P9)
0013 <sub>16</sub>	Port P9 direction register (P9D)
0014 <sub>16</sub>	Port PA (PA)
0015 <sub>16</sub>	Port PA direction register (PAD)
0016 <sub>16</sub>	Port PB (PB)
0017 <sub>16</sub>	
0018 <sub>16</sub>	Serial I/O automatic transfer data pointer (SIODP)
0019 <sub>16</sub>	Serial I/O1 control register (SIO1CON)
001A <sub>16</sub>	Serial I/O automatic transfer control register (SIOAC)
001B <sub>16</sub>	Serial I/O1 register (SIO1)
001C <sub>16</sub>	Serial I/O automatic transfer interval register (SIOAI)
001D <sub>16</sub>	Serial I/O2 control register (SIO2CON)
001E <sub>16</sub>	
001F <sub>16</sub>	Serial I/O2 register (SIO2)
0020 <sub>16</sub>	Timer 1 (T1)
0021 <sub>16</sub>	Timer 2 (T2)
0022 <sub>16</sub>	Timer 3 (T3)
0023 <sub>16</sub>	Timer 4 (T4)
0024 <sub>16</sub>	Timer 5 (T5)
0025 <sub>16</sub>	Timer 6 (T6)
0026 <sub>16</sub>	
0027 <sub>16</sub>	Timer 6 PWM register (T6PWM)
0028 <sub>16</sub>	Timer 12 mode register (T12M)
0029 <sub>16</sub>	Timer 34 mode register (T34M)
002A <sub>16</sub>	Timer 56 mode register (T56M)
002B <sub>16</sub>	PWM control register (PWMCON)
002C <sub>16</sub>	PWM register (upper)(PWMH)
002D <sub>16</sub>	PWM register (lower)(PWML)
002E <sub>16</sub>	
002F <sub>16</sub>	
0030 <sub>16</sub>	A-D control register (ADCON)
0031 <sub>16</sub>	A-D conversion register (AD)
0032 <sub>16</sub>	Port P3 segment/digit switching register (P3SDR)
0033 <sub>16</sub>	Port P0 digit/port switching register (P0DPR)
0034 <sub>16</sub>	Port P8 segment/port switching register (P8SPR)
0035 <sub>16</sub>	Key-scan blanking register (KSCN)
0036 <sub>16</sub>	FLDC mode register (FLDM)
0037 <sub>16</sub>	FLD data pointer (FLDDP)
0038 <sub>16</sub>	High-breakdown-voltage port control register (HVPC)
0039 <sub>16</sub>	
003A <sub>16</sub>	Interrupt edge selection register (INTEDGE)
003B <sub>16</sub>	CPU mode register (CUPM)
003C <sub>16</sub>	Interrupt request register 1 (IREQ1)
003D <sub>16</sub>	Interrupt request register 2 (IREQ2)
003E <sub>16</sub>	Interrupt control register 1 (ICON1)
003F <sub>16</sub>	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

## I/O PORTS

### • Direction Registers

The M3818x group microprocessors have 67 programmable I/O pins arranged in nine I/O ports (ports P1, P2, P4, P4<sub>7</sub>, P5-P8, P9<sub>0</sub>-P9<sub>3</sub> and PA ). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

### • High-Breakdown-Voltage Output Ports

The M3818x group microprocessors have four ports with high-breakdown-voltage pins (ports P0, P3, P8, P9). The high-breakdown-voltage ports have P-channel open drain output with a breakdown voltage of  $V_{CC} - 40V$ . Each pin in Ports P0, P3, and P9 has an internal pull-down resistor connected to  $V_{EE}$ . Port P8 has no internal pull-down resistors and external resistors should be used if necessary. At reset, the P-channel output transistor of each port latch is turned off, so it is forced to the level of  $V_{EE}$  by the pull-down resistor.

Writing "1" to bit 0 of the high-breakdown-voltage port control register (address 0038<sub>16</sub>) slows the transition of the output transistors to reduce transient noise. At reset, bit 0 of the high-breakdown-voltage port control register is set to "0" (strong drive).

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Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P0 <sub>0</sub> /SEG <sub>8</sub> — P0 <sub>3</sub> /DIG <sub>11</sub>	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown-voltage port control register	(1)
P0 <sub>4</sub> /SEG <sub>12</sub> — P0 <sub>7</sub> /SEG <sub>15</sub>					FLDC mode register Digit/port switching register High-breakdown-voltage port control register	(2)
P1 <sub>0</sub> —P1 <sub>7</sub>	Port P1	Input/output, individual bits	CMOS level input CMOS 3-state output			(3)
P2 <sub>0</sub> —P2 <sub>7</sub>	Port P2	Input/output, individual bits	TTL level input CMOS 3-state output			(3)
P3 <sub>0</sub> /SEG <sub>16</sub> / DIG <sub>16</sub> —P3 <sub>7</sub> / SEG <sub>23</sub> /DIG <sub>7</sub>	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/digit switching register High-breakdown-voltage port control register	(4)
P4 <sub>0</sub> /INT <sub>0</sub>	Port P4	Input	CMOS level input	External interrupt input	Interrupt edge selection register	(5)
P4 <sub>1</sub> /INT <sub>1</sub> — P4 <sub>4</sub> /INT <sub>4</sub>		Input/output, individual bits	CMOS level input CMOS 3-state output	External interrupt input	Interrupt edge selection register	(6)
P4 <sub>5</sub>				Timer output		
P4 <sub>6</sub> /T1 <sub>OUT</sub> , P4 <sub>7</sub> /T3 <sub>OUT</sub>					Timer 12 mode register Timer 34 mode register	(7)
P5 <sub>0</sub> /S <sub>IN1</sub> , P5 <sub>1</sub> /S <sub>OUT1</sub> , P5 <sub>2</sub> /S <sub>CLK1</sub> , P5 <sub>3</sub> /S <sub>RDY1</sub> / CS/S <sub>CLK12</sub>	Port P5	Input/output, individual bits	CMOS level input N-channel open-drain output	Serial I/O1 function I/O	Serial I/O1 control register	(8)
P5 <sub>4</sub> /S <sub>IN2</sub> , P5 <sub>5</sub> /S <sub>OUT2</sub> , P5 <sub>6</sub> /S <sub>CLK2</sub> , P5 <sub>7</sub> /S <sub>RDY2</sub>					Serial I/O2 control register	(9)
				Serial I/O2 function I/O	Serial I/O automatic transfer control register	(10)
P6 <sub>0</sub> /PWM <sub>0</sub>	Port P6	Input/output, individual bits	CMOS level input CMOS 3-state output	14-bit PWM output	PWM control register PWML register PWMH register	(11)
P6 <sub>1</sub> /PWM <sub>1</sub>				8-bit PWM output	Timer 56 mode register Timer 6 PWM register	(7)
P6 <sub>2</sub> /CNTR <sub>0</sub> , P6 <sub>3</sub> /CNTR <sub>1</sub>				External count input	Interrupt edge selection register	(6)
P6 <sub>4</sub> —P6 <sub>7</sub>						(3)
P7 <sub>0</sub> /AN <sub>0</sub> — P7 <sub>7</sub> /AN <sub>7</sub>	Port P7	Input/output, individual bits	CMOS level input CMOS 3-state output	A-D converter input	A-D control register	(12)
P8 <sub>0</sub> /SEG <sub>0</sub> — P8 <sub>7</sub> /SEG <sub>7</sub>	Port P8	Input/output, individual bits	CMOS level input High-breakdown-voltage P-channel open-drain output without pull-down resistor	FLD automatic display function	FLDC mode register Segment/port switching register High-breakdown-voltage port control register	(13)

Note. Make sure that the input level at each pin is either 0V or V<sub>CC</sub> during execution of the STP instruction  
If an input level is at an intermediate potential, a current will flow in the input-stage gate

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Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P9 <sub>0</sub> /SEG <sub>8</sub> — P9 <sub>3</sub> /SEG <sub>11</sub>	Port P9	Input/output, individual bits	CMOS level input High-breakdown- voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register High-breakdown- voltage port control register	(14)
P9 <sub>4</sub> /SEG <sub>12</sub> — P9 <sub>7</sub> /SEG <sub>15</sub>		Output	High-breakdown- voltage P-channel open-drain output with pull-down resistor			(15)
PA <sub>0</sub> —PA <sub>7</sub>	Port PA	Input/output, individual bits	CMOS level input CMOS 3-state output			(3)
PB <sub>0</sub> , PB <sub>1</sub>	Port PB	Input	CMOS level input			(16)

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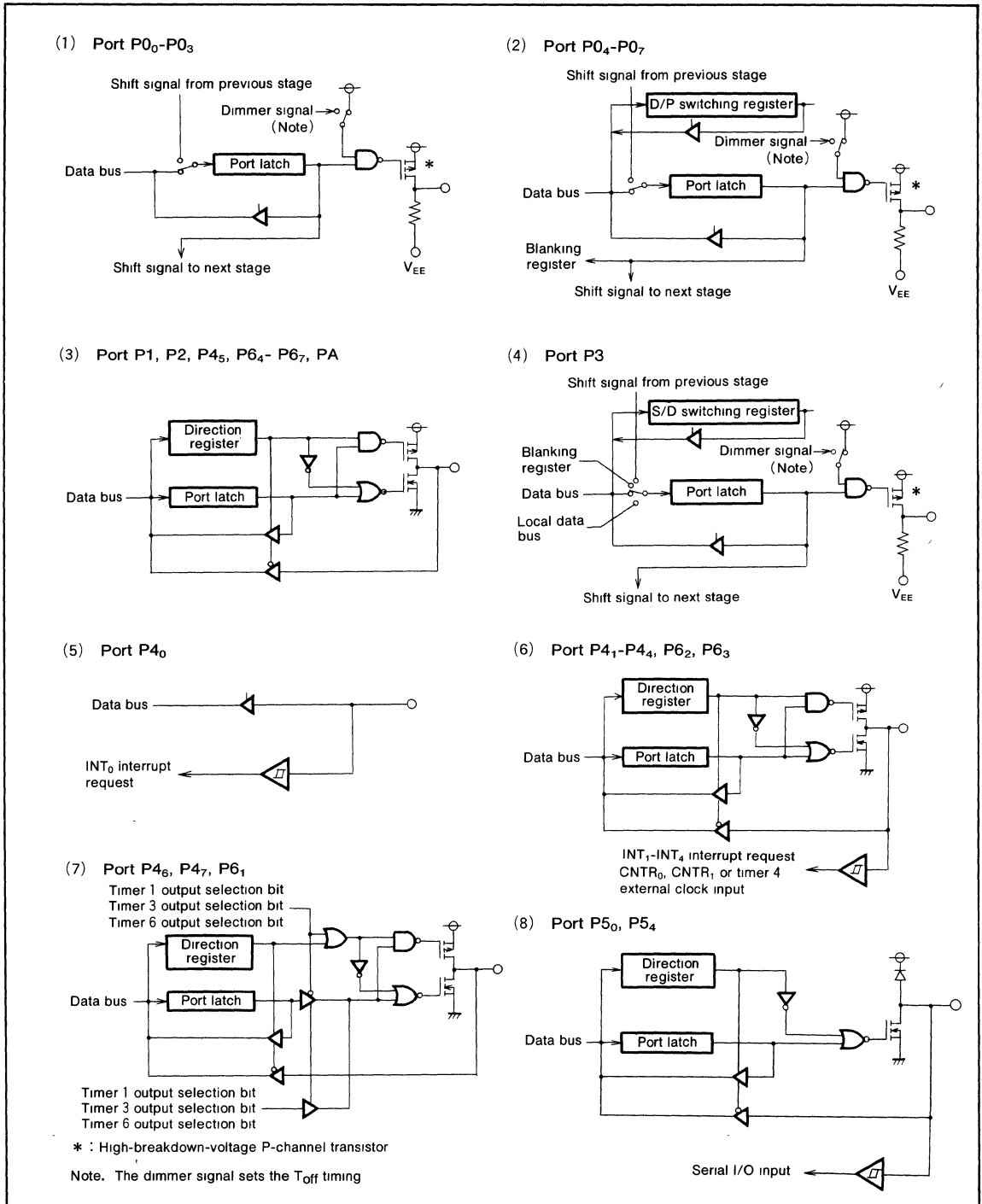


Fig. 4 Port block diagram (1)

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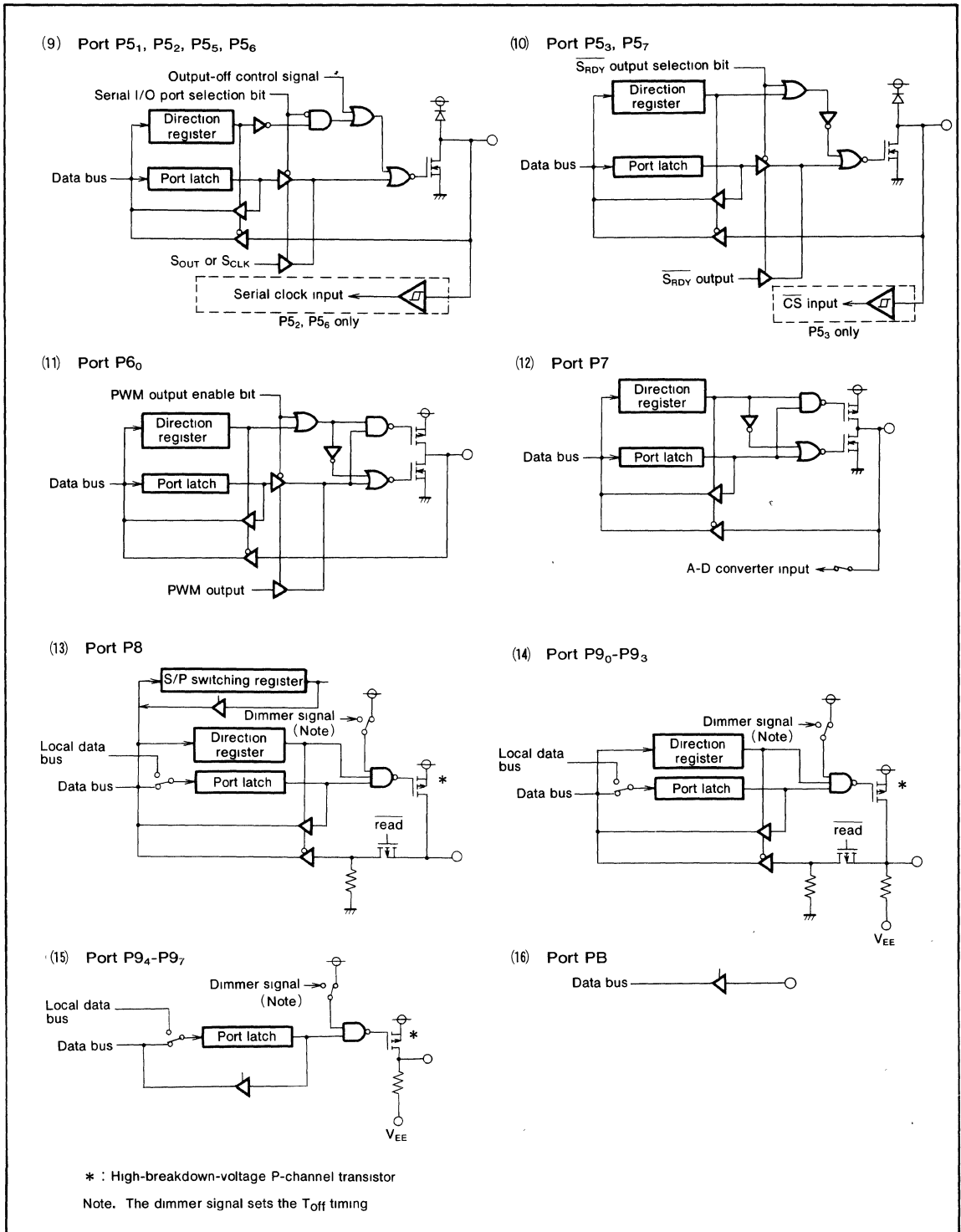


Fig. 5 Port block diagram (2)

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**INTERRUPTS**

A total of 18 source can generate interrupts: 5 external, 12 internal, and 1 software.

• **Interrupt Control**

Each interrupt is controlled by its interrupt request bit, its interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software.

The I flag disables all interrupts except for the BRK instruction interrupt.

• **Interrupt Operation**

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

• **Notes on Use**

If you will change interrupt edge selection from rising edge to falling edge, interrupt request bit will be set to "1" automatically. Therefore, please make following process;

- (1) Disable INT which is selected.
- (2) Change INT edge selection.
- (3) Clear interrupt request which is selected.
- (4) Enable INT which is selected.

**Table 1. Interrupt vector addresses and priorities**

Interrupt Cause	Priority	Vector Address (Note 1)		Interrupt Request Generation Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD <sub>16</sub>	FFFC <sub>16</sub>	At reset	Non-maskable
INT <sub>0</sub>	2	FFFB <sub>16</sub>	FFFA <sub>16</sub>	At detection of either rising or falling edge of INT <sub>0</sub> input	External interrupt (active edge selectable)
INT <sub>1</sub>	3	FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>1</sub> input	External interrupt (active edge selectable)
INT <sub>2</sub>	4	FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>2</sub> input	External interrupt (active edge selectable)
Serial I/O1	5	FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	At end of data transfer	Valid when serial I/O normal mode is selected
Serial I/O automatic transfer				At end of final data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	At end of data transfer	
Timer 1	7	FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	At timer 1 overflow	
Timer 2	8	FFEF <sub>16</sub>	FFEE <sub>16</sub>	At timer 2 overflow	STP release timer overflow
Timer 3	9	FFED <sub>16</sub>	FFEC <sub>16</sub>	At timer 3 overflow	
Timer 4	10	FFEB <sub>16</sub>	FFEA <sub>16</sub>	At timer 4 overflow	
Timer 5	11	FFE9 <sub>16</sub>	FFE8 <sub>16</sub>	At timer 5 overflow	
Timer 6	12	FFE7 <sub>16</sub>	FFE6 <sub>16</sub>	At timer 6 overflow	
INT <sub>3</sub>	13	FFE5 <sub>16</sub>	FFE4 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>3</sub> input	External interrupt (active edge selectable)
INT <sub>4</sub>	14	FFE3 <sub>16</sub>	FFE2 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>4</sub> input	External interrupt valid when INT <sub>4</sub> interrupt is selected (active edge selectable)
A-D converter				At end of A-D conversion	Valid when A-D interrupt is selected
FLD blanking	15	FFE1 <sub>16</sub>	FFE0 <sub>16</sub>	At fall of final digit	Valid when FLD blanking interrupt is selected
FLD digit				At rise of each digit	Valid when FLD digit interrupt is selected
BRK instruction	16	FFDD <sub>16</sub>	FFDC <sub>16</sub>	At BRK instruction execution	Non-maskable software interrupt

Note 1. Vector addresses contain interrupt jump destination addresses

2. Reset function in the same way as an interrupt with the highest priority

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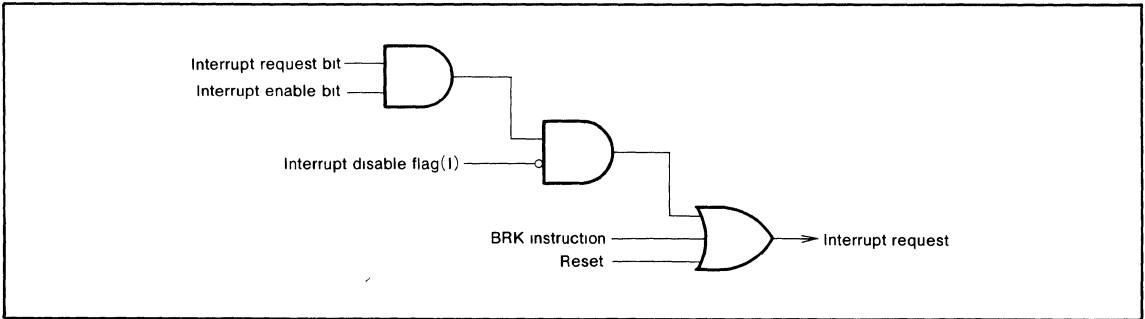


Fig. 6 Interrupt control

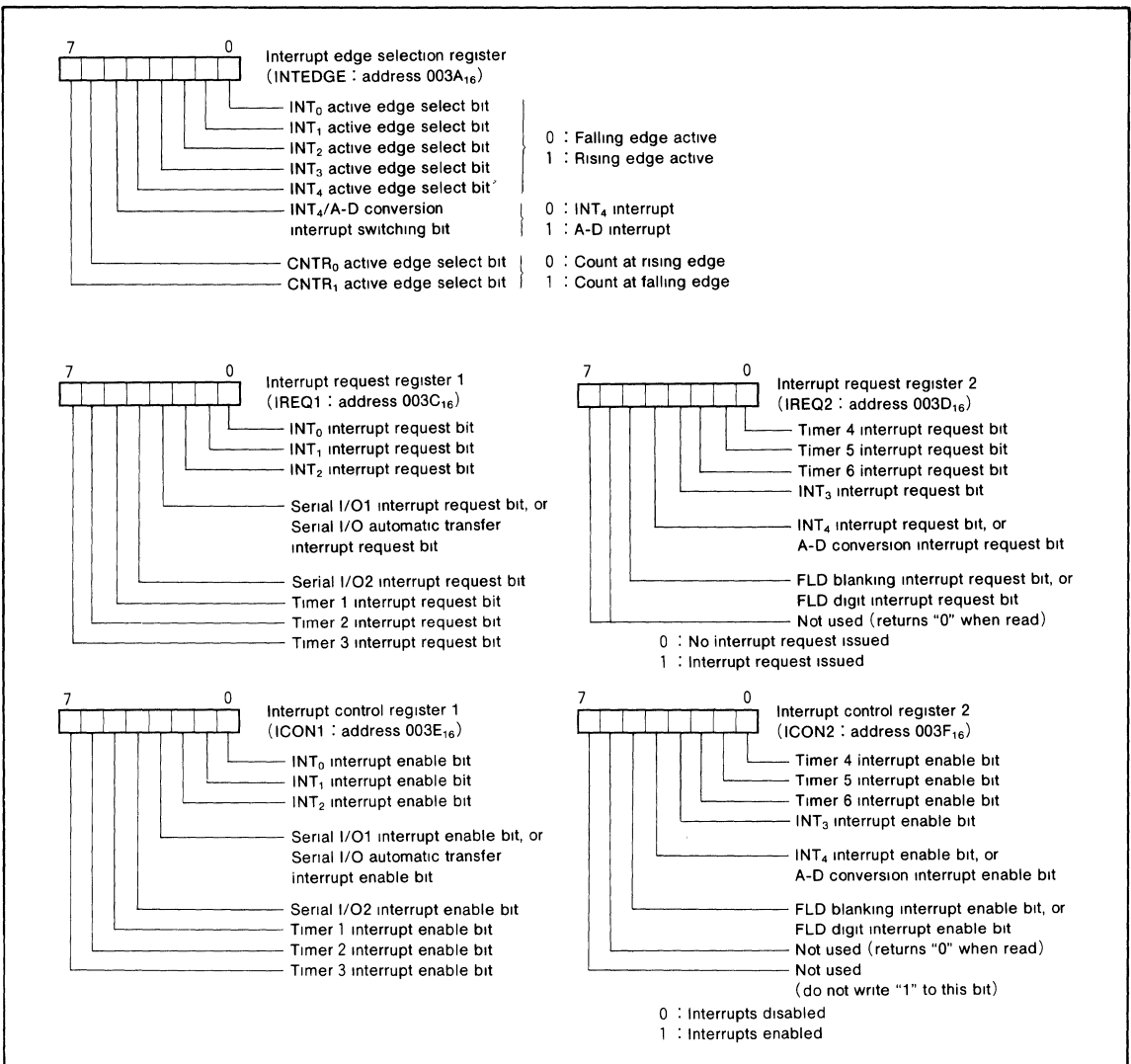


Fig. 7 Structure of interrupt-related registers

## TIMERS

Microcomputers of the M3818x group have six built-in timers. The timers count down. Once a timer reaches  $00_{16}$ , the next count pulse loads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1. Each timer also has a stop bit that stops the count of that timer when it is set to "1".

Note that the system clock  $\phi$  can be set to either high-speed mode or low-speed mode by the CPU mode register.

### • Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register.

Timer 1 can also output a rectangular waveform from the  $P4_6/T1_{OUT}$  pin. The waveform changes polarity each time timer 1 overflows.

The active edge of the external signal  $CNTR_0$  can be set by the interrupt edge selection register.

When the chip is reset or the STP instruction is executed, all bits of the timer 12 mode register are cleared, timer 1 is set to  $FF_{16}$ , and timer 2 is set to  $01_{16}$ .

### • Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register.

Timer 3 can also output a rectangular waveform from the  $P4_7/T3_{OUT}$  pin. The waveform changes polarity each time timer 3 overflows.

The active edge of the external signal  $CNTR_1$  can be set by the interrupt edge selection register.

### • Timer 5 and Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

Timer 6 can also output a rectangular waveform from the  $P6_7/PWM_1$  pin. The waveform changes polarity each time timer 6 overflows.

### • Timer 6 PWM<sub>1</sub> Mode

Timer 6 can also output a rectangular waveform of  $n$  cycles high and  $m$  cycles low. The  $n$  is the value set in timer latch 6 (address  $0025_{16}$ ) and  $m$  is the value in the timer 6 PWM register (address  $0027_{16}$ ). If  $n$  is "0", the  $PWM_1$  output is "L", if  $m$  is "0" and  $n$  is not "0", then the  $PWM_1$  output is "H". In PWM mode, interrupts are generated at the rising edge of the  $PWM_1$  output.



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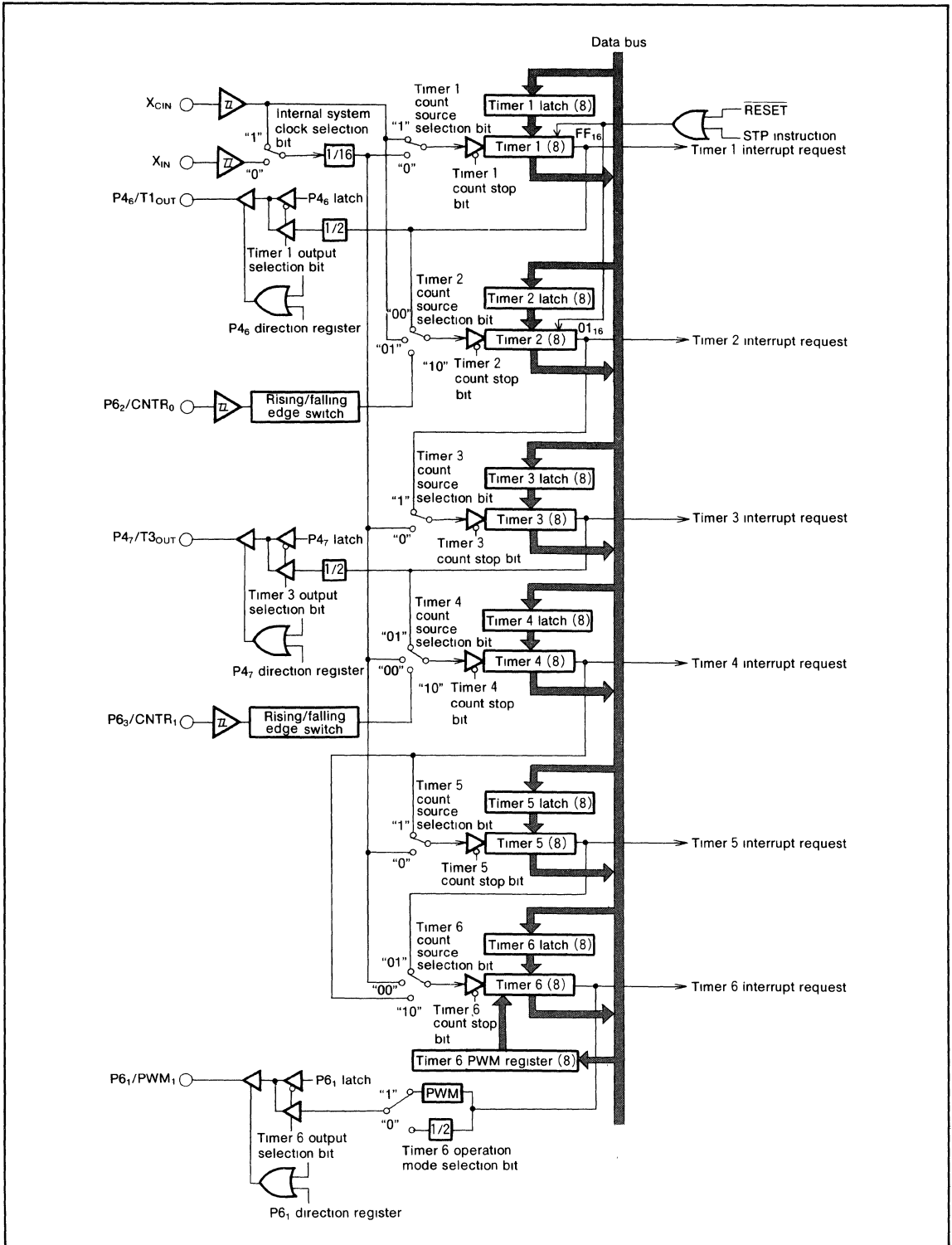


Fig. 8 Timer block diagram

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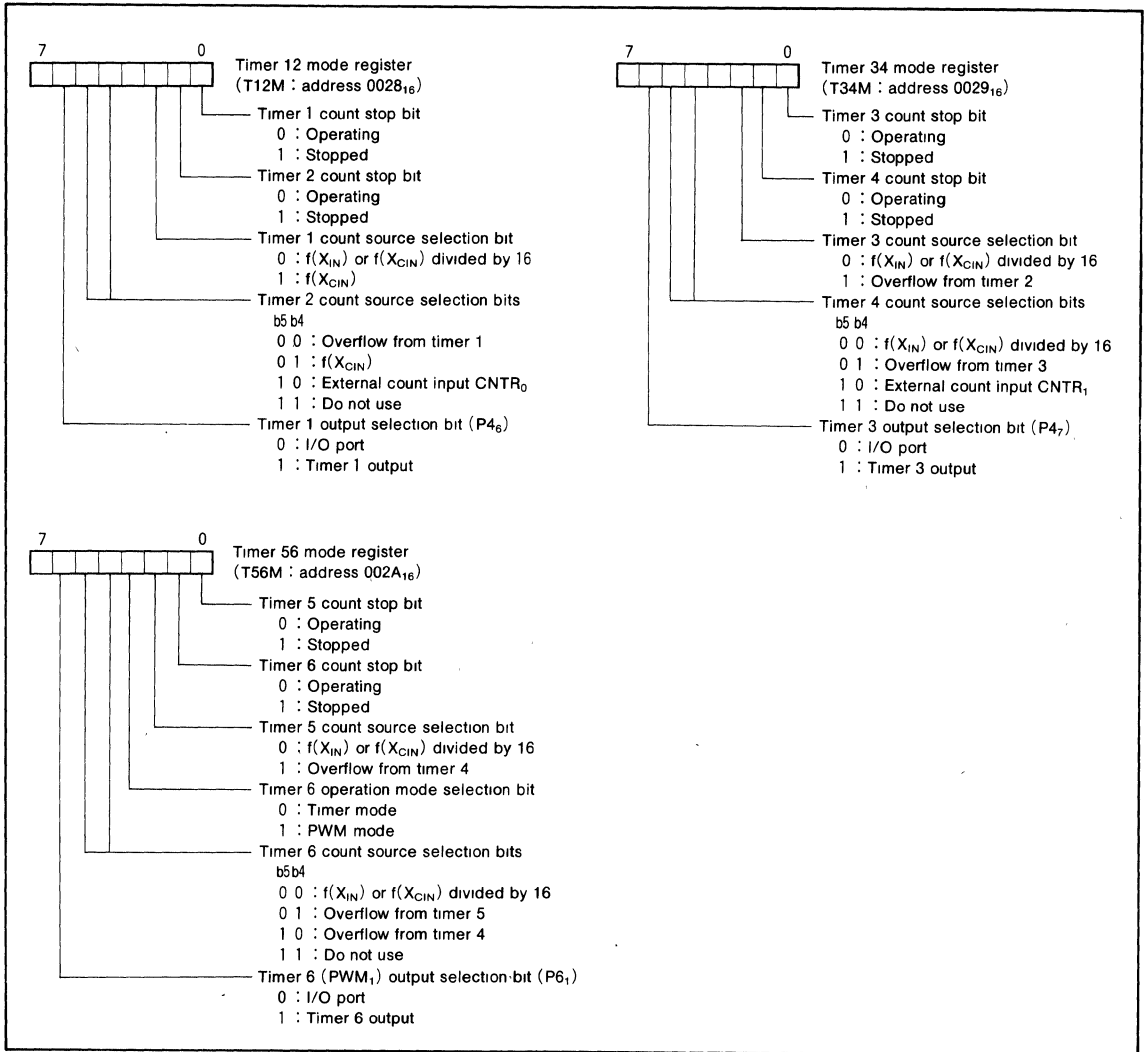


Fig. 9 Structure of timer-related registers

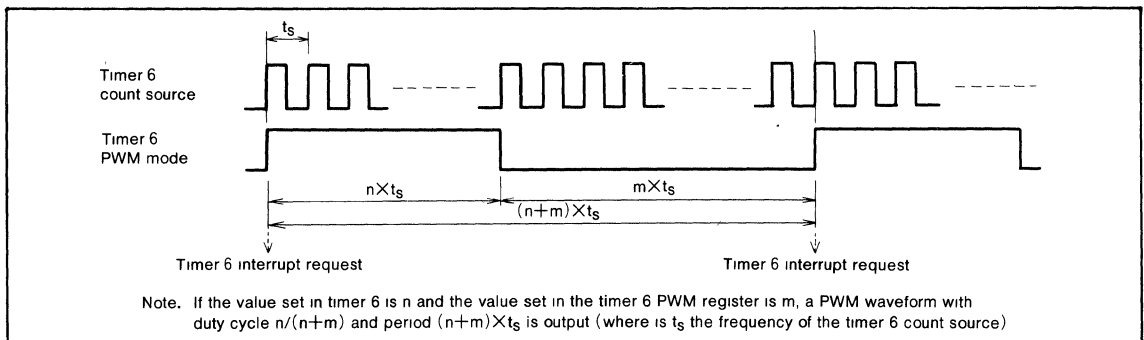


Fig. 10 Timing in timer 6 PWM<sub>1</sub> mode

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SERIAL I/O

Microcomputers of the M3818x group have two built-in 8-bit clock synchronized serial I/O channels (serial I/O1 and serial I/O2).

Serial I/O1 has a built-in automatic transfer function. Normal serial operation can be set via the serial I/O automatic transfer control register (address 001A<sub>16</sub>).

Serial I/O2 can only be used in normal operation mode.

The I/O pins of the serial I/O function also operate as I/O port P5, and their operation is selected by the serial I/O control registers (addresses 0019<sub>16</sub> and 001D<sub>16</sub>).

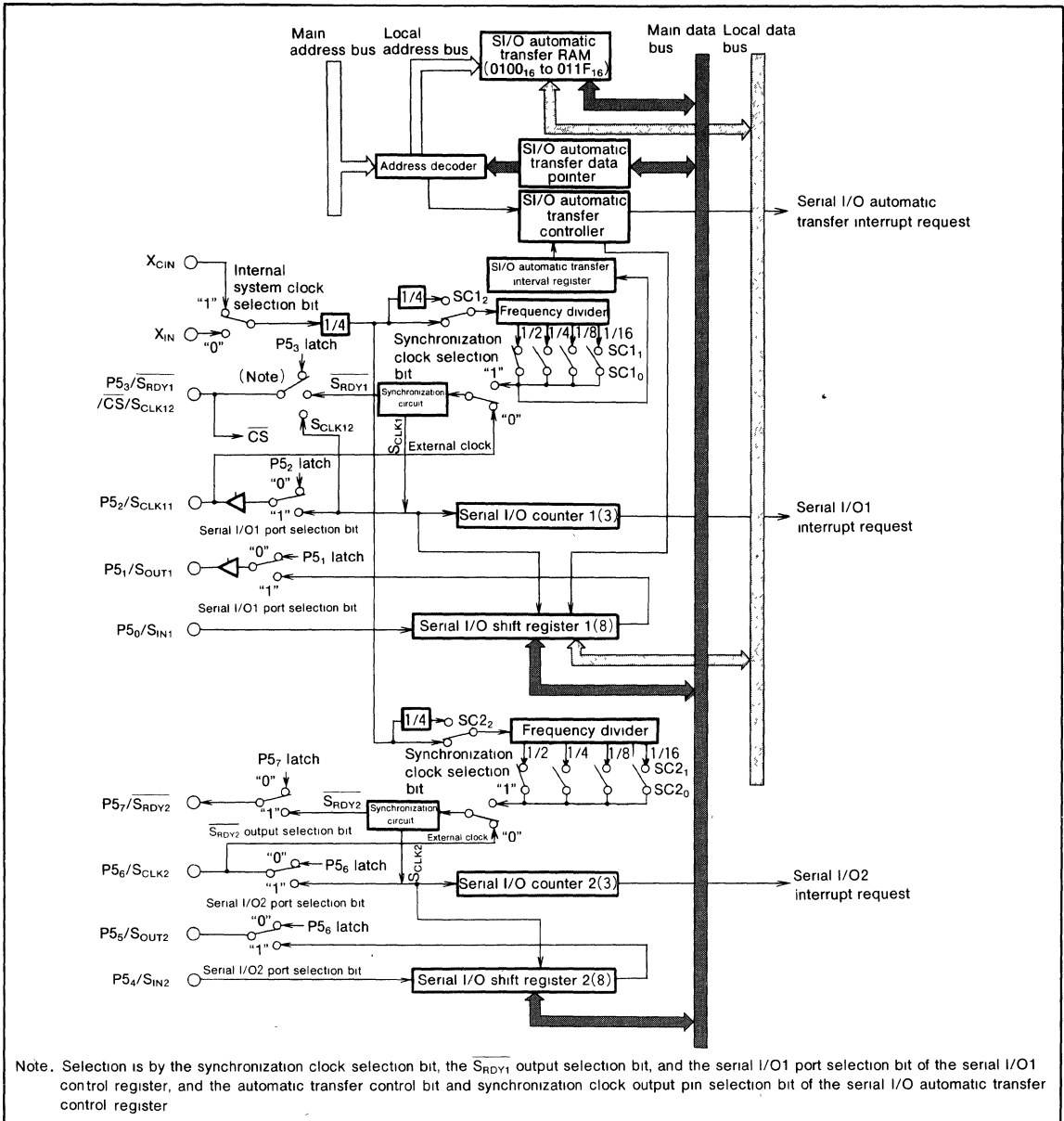


Fig. 11 Serial I/O block diagram

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(Serial I/O Control Registers) SIO1CON, SIO2CON

Each of the serial I/O control registers (addresses 0019<sub>16</sub> and 001D<sub>16</sub>) contains seven bits that select various control parameters of the serial I/O function.

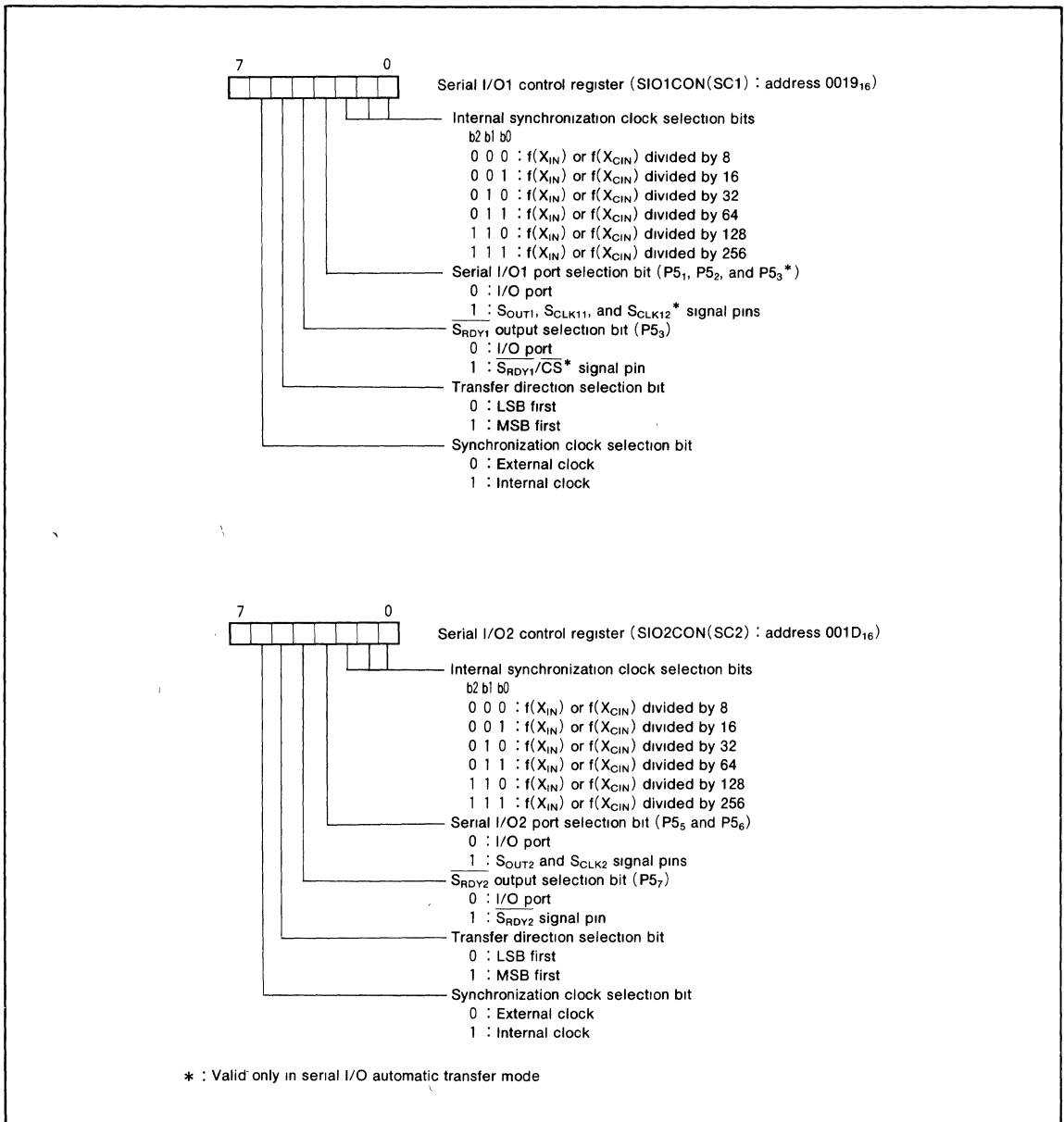


Fig. 12 Structure of serial I/O control registers

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(1) Operation in Normal Serial I/O Mode

Either an internal clock or an external clock can be selected as the synchronization clock for serial I/O transfer. A dedicated divider is built-in as the internal clock, giving a choice of six clocks.

If internal clock is selected, transfer start is activated by a write signal to a serial I/O register (address 001B<sub>16</sub> or 001F<sub>16</sub>). After eight bits have been transferred, the S<sub>OUT</sub> pin goes to high impedance.

If external clock is selected, the clock must be controlled externally because the contents of the serial I/O register continue to shift while the transfer clock is input. In this case, note that the S<sub>OUT</sub> pin does not go to high impedance at the completion of data transfer. The interrupt request bit is set at the end of the transfer of eight bits, regardless of whether the internal or external clock is selected.

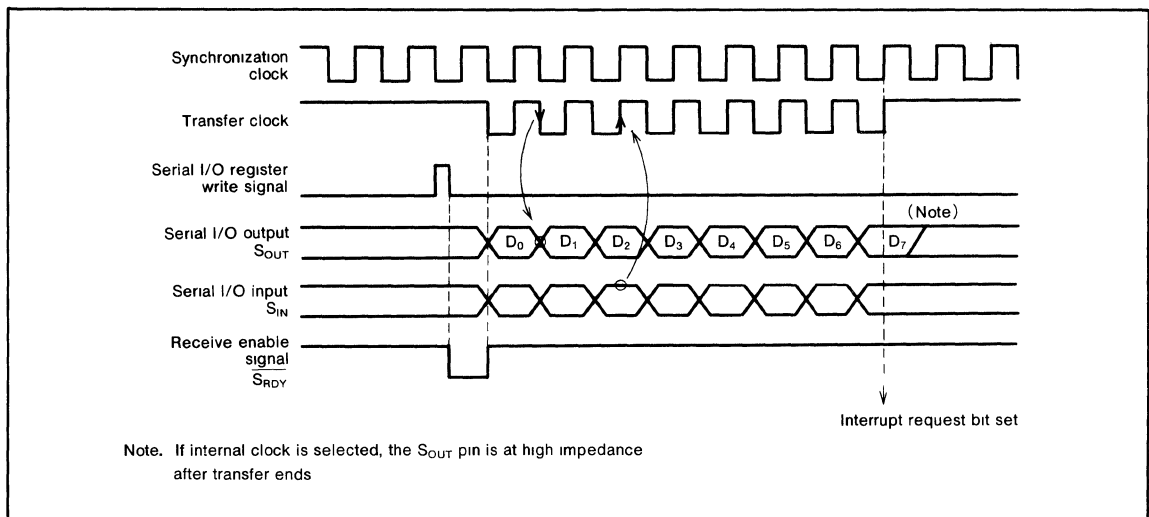


Fig. 13 Serial I/O timing in normal mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode

The serial I/O1 function has an automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address 001A<sub>16</sub>).

The following memory spaces are added to the circuits used for the serial I/O1 function in ordinary mode, to enable automatic transfer mode:

- 32 bytes of serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O control register (address 0019<sub>16</sub>) in the same way as for ordinary mode. However, note that if external clock is selected and bit 4 (the S<sub>RDY1</sub> output selection bit) of the serial I/O1 control register is set to "1", port P5<sub>3</sub> becomes the CS input pin.

(Serial I/O Automatic Transfer Control Register) SIOAC

The serial I/O automatic transfer control register (address 001A<sub>16</sub>) contains four bits that select various control parameters for automatic transfer.

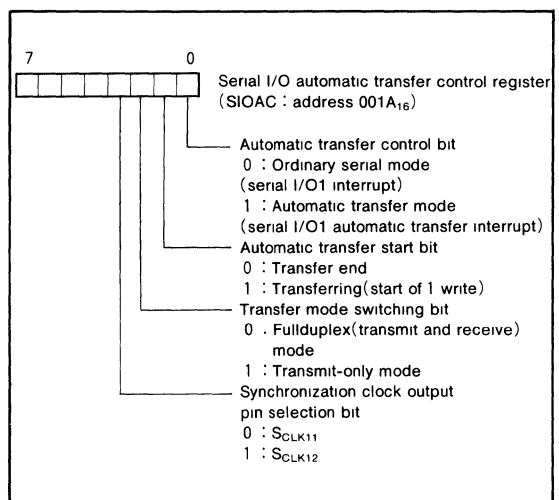


Fig. 14 Structure of serial I/O automatic transfer control register

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**(Serial I/O Automatic Transfer Data Pointer) SIODP**

The serial I/O automatic transfer data pointer (address 0018<sub>16</sub>) contains five bits that indicate addresses in serial I/O automatic transfer RAM (each address in memory is actually the value in the serial I/O automatic transfer data pointer plus 0100<sub>16</sub>).

Set the serial I/O automatic transfer data pointer to (the number of transfer data - 1), to specify the storage position of the start of data.

• **Serial I/O Automatic Transfer RAM**

The serial I/O automatic transfer RAM is the 32 bytes from address 0100<sub>16</sub> to address 011F<sub>16</sub>.

• **Setting of Serial I/O Automatic Transfer Data**

When data is stored in the serial I/O automatic transfer RAM, it is stored with the start of the data at the address set by the serial I/O automatic transfer data pointer and the end of the data at address 0100<sub>16</sub>.

**(Serial I/O Automatic Transfer Interval Register) SIOAI**

The serial I/O automatic transfer interval register (address 001C<sub>16</sub>) consists of a 5-bit counter that determines the transfer interval  $T_i$  during automatic transfer.

If a value  $n$  is written to the serial I/O automatic transfer interval register, a value of  $T_i = (n + 2) \times T_c$  is generated, where  $T_c$  is the length of one bit of the transfer clock. However, note that this transfer interval setting is only valid when internal clock has been selected as the clock source.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0100 <sub>16</sub>								
0101 <sub>16</sub>								
0102 <sub>16</sub>								
⋮								
011D <sub>16</sub>								
011E <sub>16</sub>								
011F <sub>16</sub>								

Fig. 15 Bit allocation of serial I/O automatic transfer RAM

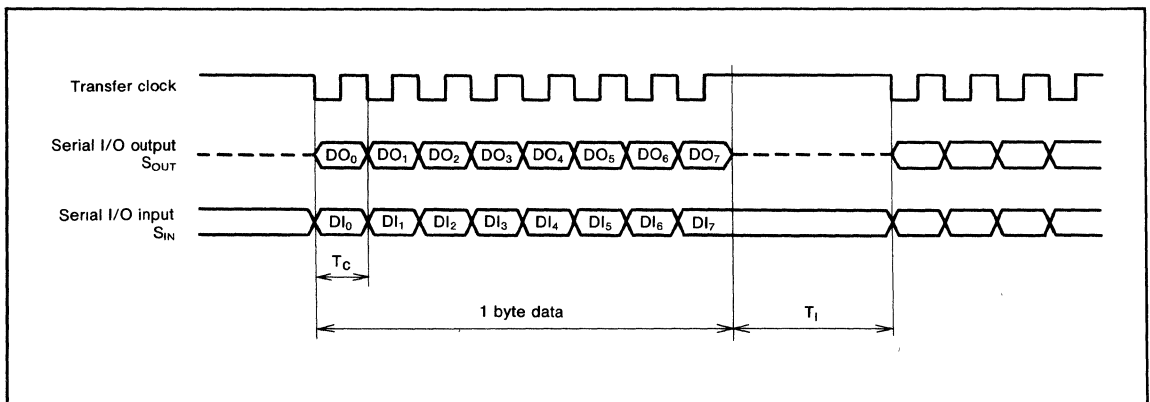


Fig. 16 Serial I/O automatic transfer interval timing

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- Setting of Serial I/O Automatic Transfer Timing**  
 Use the serial I/O1 control register (address 0019<sub>16</sub>) and the serial I/O automatic transfer interval register (address 001C<sub>16</sub>) to set the timing of serial I/O automatic transfer.  
 The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval.  
 This setting of transfer interval is valid only when internal clock is selected as the clock source.
- Start of Serial I/O Automatic Transfer**  
 Automatic transfer mode is set by writing "1" to bit 0 of the serial I/O automatic transfer control register (address 001A<sub>16</sub>), then automatic transfer starts when "1" is written to that bit. Bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" to it is one way to end automatic transfer.
- Operation in Serial I/O Automatic Transfer Modes**  
 There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes

**(2.1) Operation in Full Duplex Mode**  
 In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is sent in sequence and simultaneously receive data is written to the automatic transfer RAM, in accordance with the serial I/O automatic transfer data pointer.  
 The transfer timing of each bit is the same as in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted. If internal clock is selected, the transfer clock remains at "H" for the time set by the serial I/O automatic transfer interval register, then the data at the next address indicated by the serial I/O automatic transfer data pointer is transferred. If external clock is selected, the setting of the automatic transfer interval register is invalid, so the user must ensure that the transfer clock is controlled externally.  
 Data transfer ends when the contents of the serial I/O automatic transfer pointer reach "00<sub>16</sub>". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

**(2.2) Operation in Transmit-Only Mode**  
 The operation in transmit-only mode is the same as that in full duplex mode, except that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

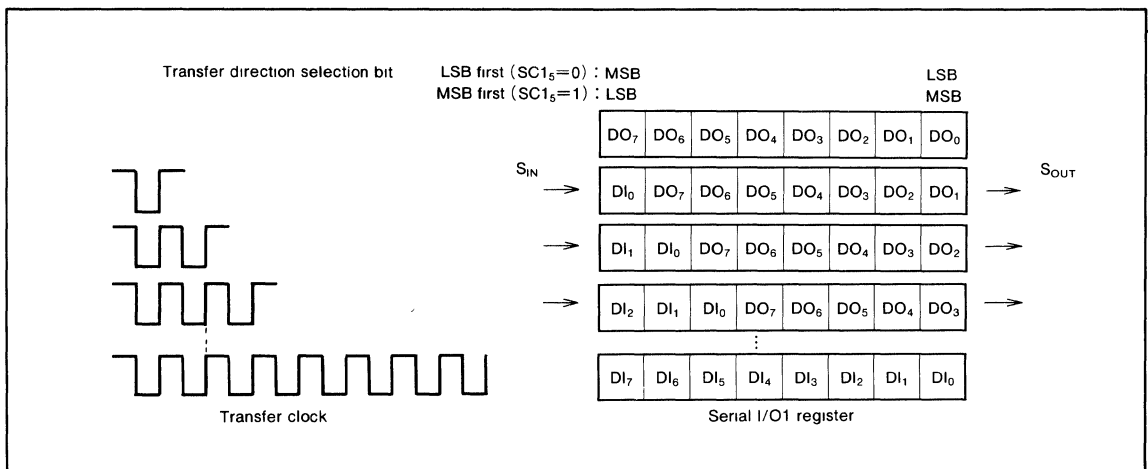


Fig. 17 Serial I/O1 register in full duplex mode

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(2.3) If Internal Clock is Selected

If internal clock is selected, the  $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$  pin can be used as the  $\overline{S_{RDY1}}$  pin by setting the  $SC1_4$  bit to "1". If internal clock is selected, the  $P5_3$  pin can be used as the synchronization clock output pin  $S_{CLK12}$  by setting the  $SIOAC_3$  bit to "1". In this case, the  $S_{CLK11}$  pin is at high impedance.

Select the function of the  $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$  and  $P5_2/S_{CLK11}$  pins by setting bit 3 ( $SC1_3$ ), bit 4 ( $SC1_4$ ), and bit 6 ( $SC1_6$ ) of the serial I/O control register (address  $0019_{16}$ ) and bit 3 ( $SIOAC_3$ ) of the serial I/O automatic transfer control register (address  $001A_{16}$ ). (See Table 2.)

If using the  $S_{CLK11}$  and  $S_{CLK12}$  pins for switching, set the  $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$  pin to  $P5_3$  by setting the  $SC1_4$  bit to "0", and set the  $P5_3$  direction register to input mode. Make sure that the  $SIOAC_3$  bit is switched after automatic transfer is completed, while the transfer clock is still "H".

Table 2.  $S_{CLK11}$  and  $S_{CLK12}$  selection

$SC1_6$	$SC1_4$	$SC3_3$	$SIOAC_3$	$P5_2/S_{CLK11}$	$P5_3/S_{CLK12}$
1	0	1	0	$S_{CLK11}$	$P5_3$
			1	High impedance	$S_{CLK12}$

Note.  $SC1_3$ : Serial I/O port selection bit  
 $SC1_4$ :  $\overline{S_{RDY1}}$  output selection bit  
 $SC1_6$ : Synchronization clock selection bit  
 $SIOAC_3$ : Synchronization clock output pin selection bit

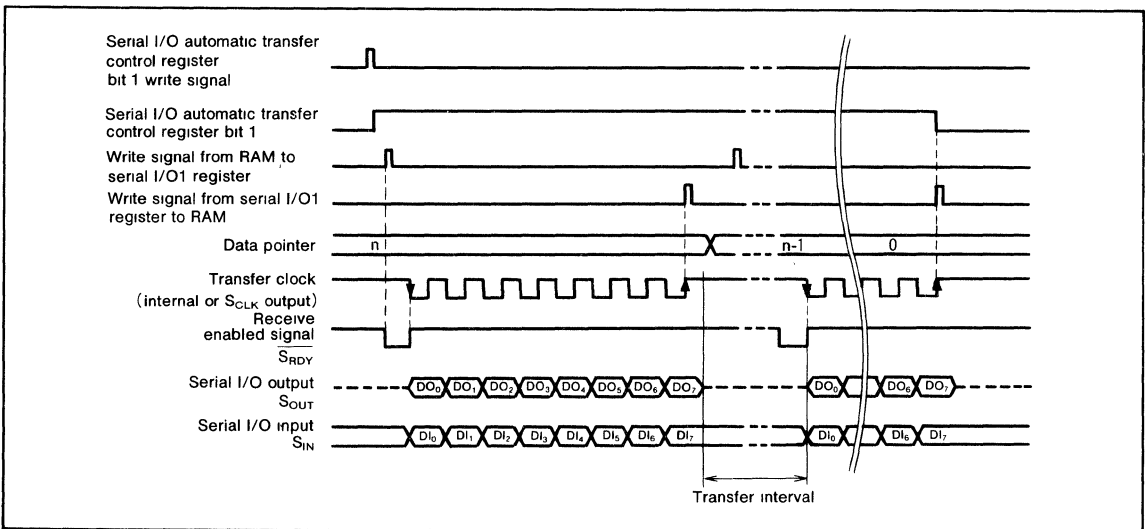


Fig. 18 Timing during serial I/O automatic transfer (internal clock selected,  $\overline{S_{RDY}}$  used)

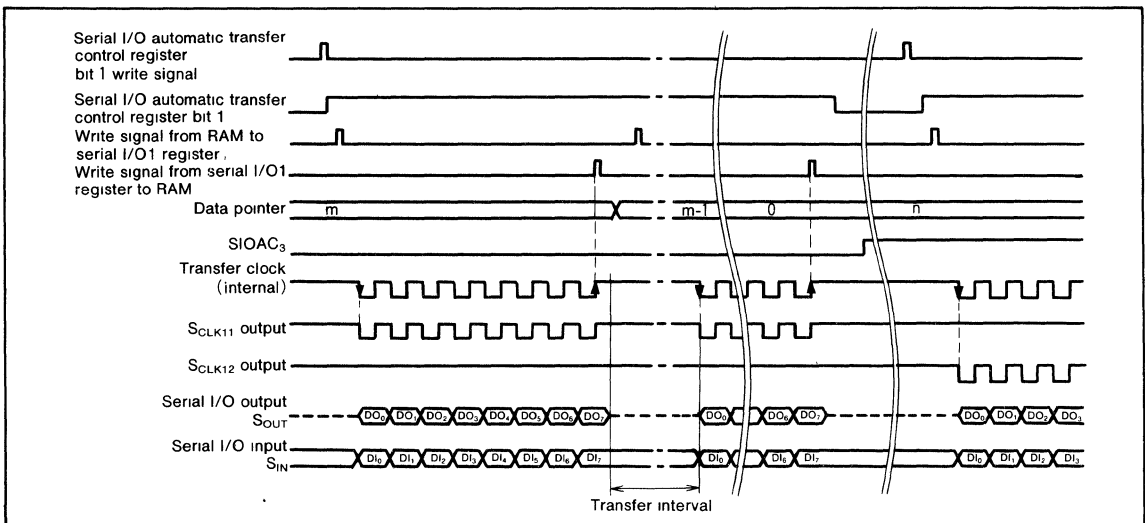


Fig. 19 Timing during serial I/O automatic transfer (internal clock selected,  $S_{CLK11}$  and  $S_{CLK12}$  used)



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**(2.4) If External Clock is Selected**

If an external clock is selected, the internal clock and the transfer interval set by the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin  $S_{OUT}$  and the internal transfer clock can be controlled from the outside by setting the  $\overline{S_{RDY1}}$  and  $\overline{CS}$  (input) pins.

When the  $\overline{CS}$  input is "L", the  $S_{OUT}$  pin and the internal transfer clock are enabled. When the  $\overline{CS}$  input is "H", the  $S_{OUT}$  pin is at high impedance and the internal transfer clock is at "H".

Select the function of the  $P5_3/\overline{S_{RDY1}}/\overline{CS}/S_{CLK12}$  pin by setting bit 4 ( $SC1_4$ ) and bit 6 ( $SC1_6$ ) of the serial I/O1 control register (address  $0019_{16}$ ) and bit 0 ( $SIOAC_0$ ) of the serial I/O automatic transfer control register (address  $001A_{16}$ ).

Make sure that the  $\overline{CS}$  pin switches from "L" to "H" or from "H" to "L" while the transfer clock ( $S_{CLK}$  input) is "H" after one byte of data has been transferred

If external clock is selected, make sure that the external clock goes "L" after at least nine cycles of the internal system clock  $\phi$  after the start bit is set. Leave at least 11 cycles of the system clock  $\phi$  free for the transfer interval after one byte of data has been transferred.

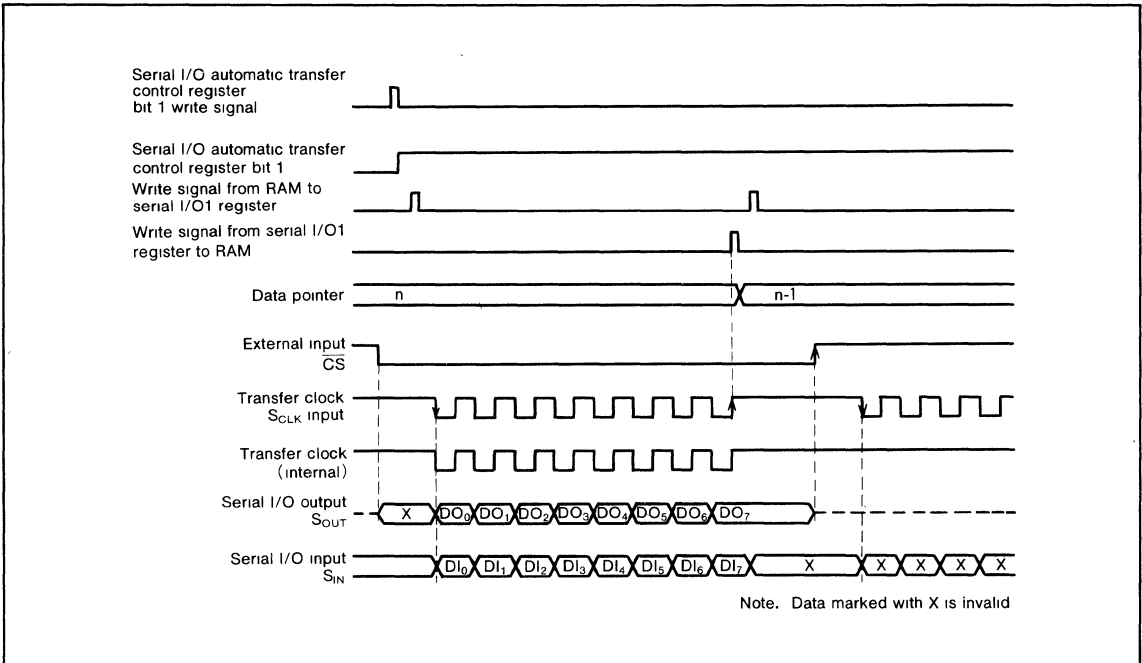
If  $\overline{CS}$  input is not being used, note that the  $S_{OUT}$  pin will not go high impedance, even after transfer is completed.

If  $\overline{CS}$  input is not being used, or if  $\overline{CS}$  is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer. (Note that the automatic transfer interrupt request bit is set and bit 1 of the automatic transfer register is cleared at the point at which the specified number of bytes of data have been transferred.)

**Table 3.  $P5_3/\overline{S_{RDY1}}/\overline{CS}$  selection**

$SC1_6$	$SC1_4$	$SIOAC_0$	$P5_3/\overline{S_{RDY1}}/\overline{CS}$
0	0	X	$P5_3$
	1	0	$\overline{S_{RDY1}}$
		1	$\overline{CS}$

Note.  $SC1_4$  :  $\overline{S_{RDY1}}$  output selection bit  
 $SC1_6$  : Synchronization clock selection bit  
 $SIOAC_0$  : Automatic transfer control bit



**Fig. 20 Timing during serial I/O automatic transfer (external clock selected)**

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**PULSE WIDTH MODULATION (PWM) OUTPUT CIRCUIT**

Microcomputers of the M3818x group have a PWM function with a 14-bit resolution. When the oscillation frequency  $X_{IN}$  is 4MHz, the minimum resolution bit width is 500ns and the cycle period is 8192 $\mu$ s. The PWM timing generator supplies a PWM control signal based on a signal that is half the frequency of the  $X_{IN}$  clock.

The explanation in the rest of this data sheet assumes  $X_{IN}$  = 4MHz.

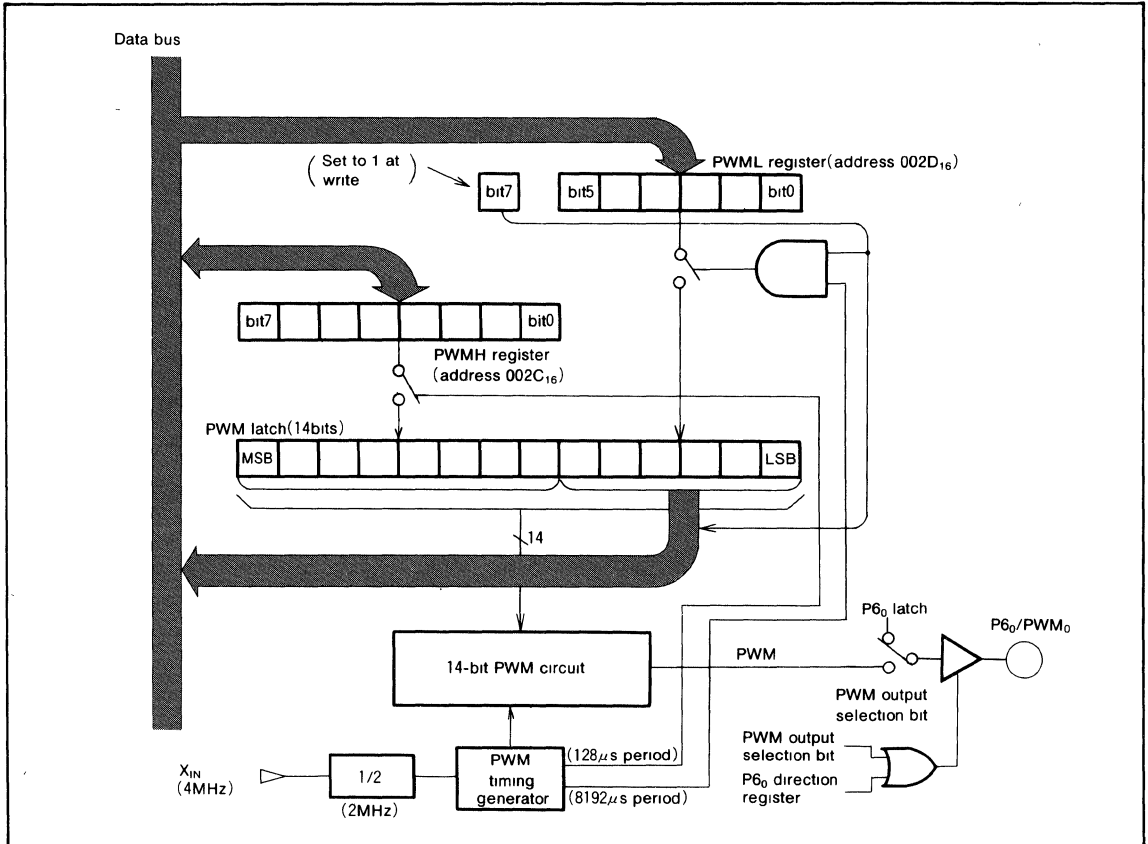


Fig. 21 PWM block diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

(1) Data Set-up

The PWM output pin also functions as port P6<sub>0</sub>. Set port P6<sub>0</sub> to be the PWM output pin by setting bit 0 of the PWM mode register (address 002B<sub>16</sub>). The upper eight bits of output data are set in the upper PWM register PWMH (address 002C<sub>16</sub>) and the lower six bits are set in the lower PWM register PWML (address 002D<sub>16</sub>).

(2) Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 8192 $\mu$ s), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 128 $\mu$ s). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0".

**Table 4. Relationship between lower 6 bits of data and period set by the ADD bit**

Lower 6 Bits of Data(PWML)	Sub-periods $t_m$ Lengthened ( $m=0$ to 63)
0 0 0 0 0 0 <sup>LSB</sup>	None
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

(3) PWM Operation

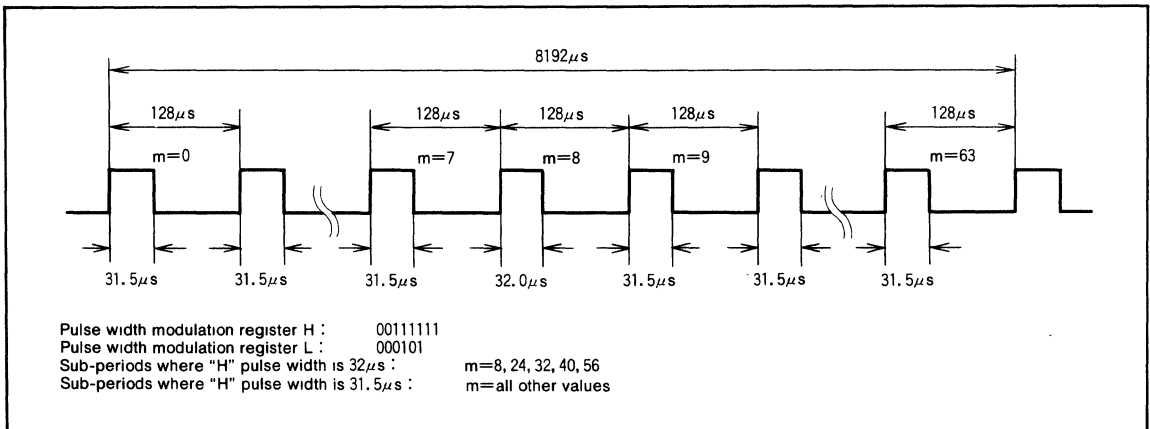
The timing of the 14-bit PWM function is shown in Fig. 24. The 14-bit PWM data is divided into the lower six bits and the upper eight bits in the PWM latch.

The upper eight bits of data determine how long an "H"-level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period is  $256 \times \tau$  (128 $\mu$ s) long. The signal is "H" for a length equal to  $N$  times  $\tau$ , where  $\tau$  is the minimum resolution (500ns).

The contents of the lower six bits of data enable the lengthening of the high signal by  $\tau$  (500ns). As shown in Fig. 21, the six bits of PWML determine which sub-cycles are lengthened.

As shown in Fig. 24, the leading edge of the pulse is lengthened. By changing the length of specific sub-periods instead of simply changing the "H" duration, an accurate waveform can be duplicated without the use of complex external filters.

For example, if the upper eight bits of the 14-bit data are 03<sub>16</sub> and the lower six bits are 05<sub>16</sub>, the length of the "H"-level output in sub-periods  $t_8, t_{24}, t_{32}, t_{40}$ , and  $t_{56}$  is  $4\tau$ , and its length  $3\tau$  in all other sub-periods.



**Fig. 22 PWM timing**

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

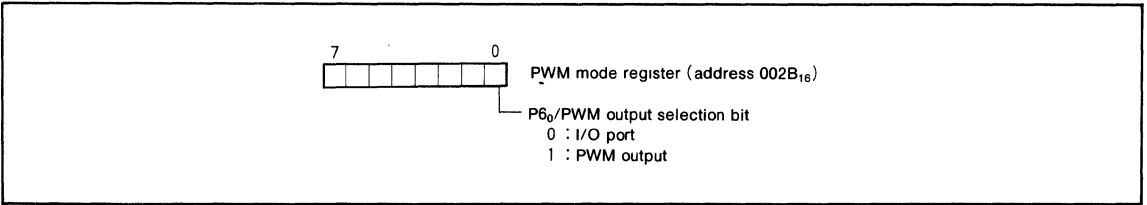


Fig. 23 Structure of PWM mode register

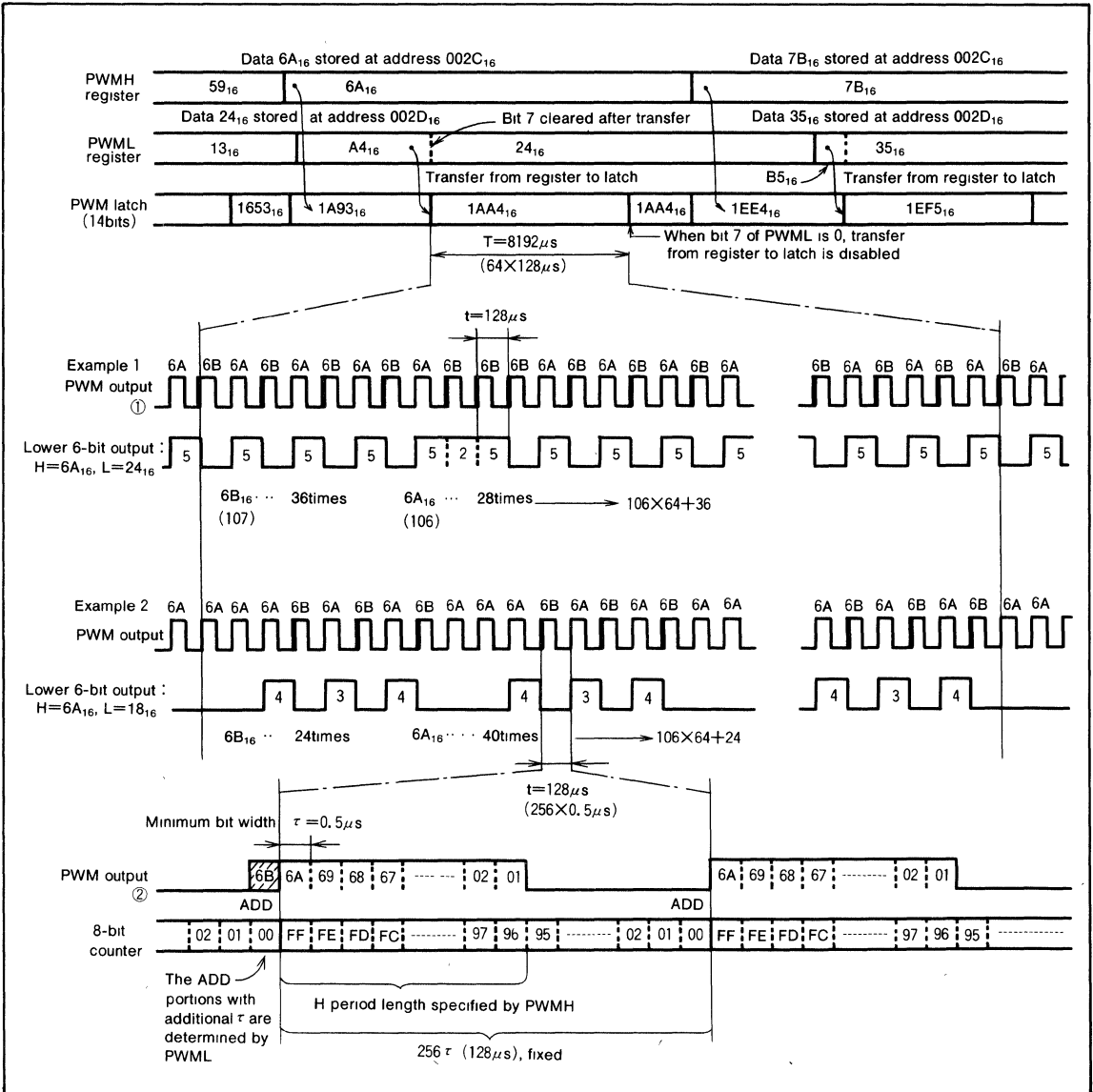


Fig. 24 14-bit PWM timing

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**A-D CONVERTER**

The functional blocks of the A-D converter are described below.

**[A-D Conversion Register] AD**

The A-D conversion register is a read-only register that contains the result of an A-D conversion. This register should not be read during an A-D conversion.

**[A-D Control Register] ADCON**

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion.

**[Comparison Voltage Generator]**

The comparison voltage generator divides the voltage between  $V_{SS}$  and  $V_{REF}$  by 256, and outputs the divided voltages.

**[Channel Selector]**

The channel selector selects one of the input ports  $P7_7/AN_7$  to  $P7_0/AN_0$ .

**[Comparator and Control Circuit]**

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set  $f(X_{IN})$  to at least 500kHz during A-D conversion.

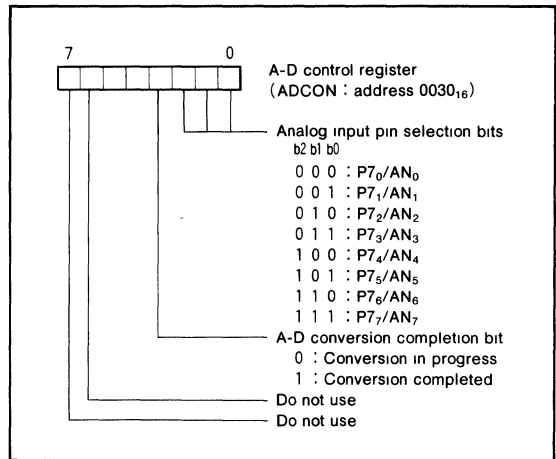


Fig. 25 Structure of A-D control register

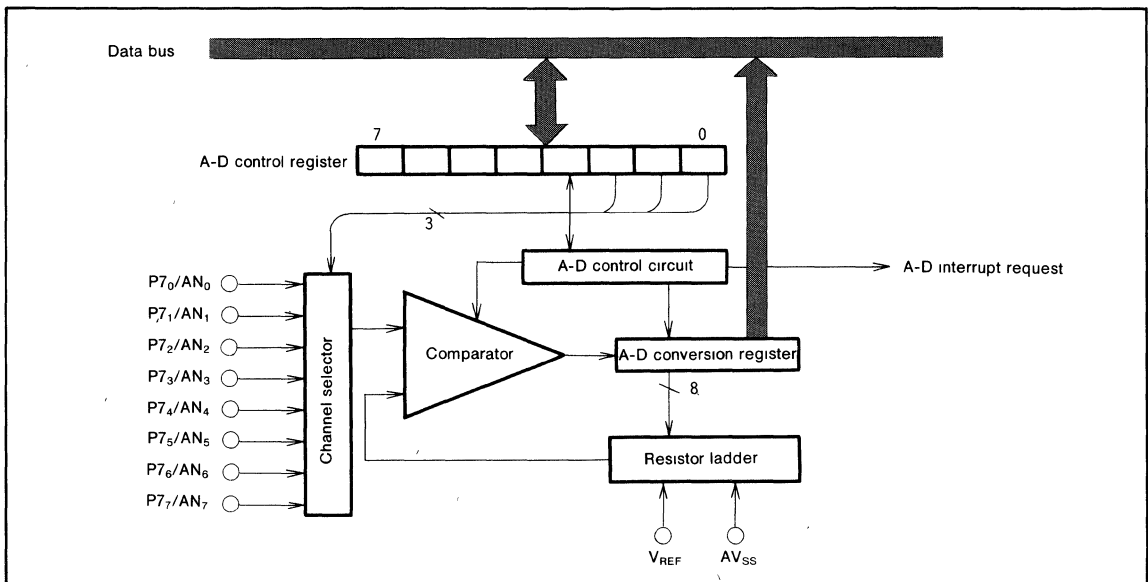


Fig. 26 A-D converter block diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**FLD CONTROLLER**

Microcomputers of the M3818x group have fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 24 pins for segments
- 16 pins for digits
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register

- Port P3 segment/digit switching register
- Port P0 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- 48-byte FLD automatic display RAM

Eight to twenty-four pins can be used as segment pins and four to sixteen pins can be used as digit pins.

Note that only 32 pins (maximum) can be used as segment and digit pins.

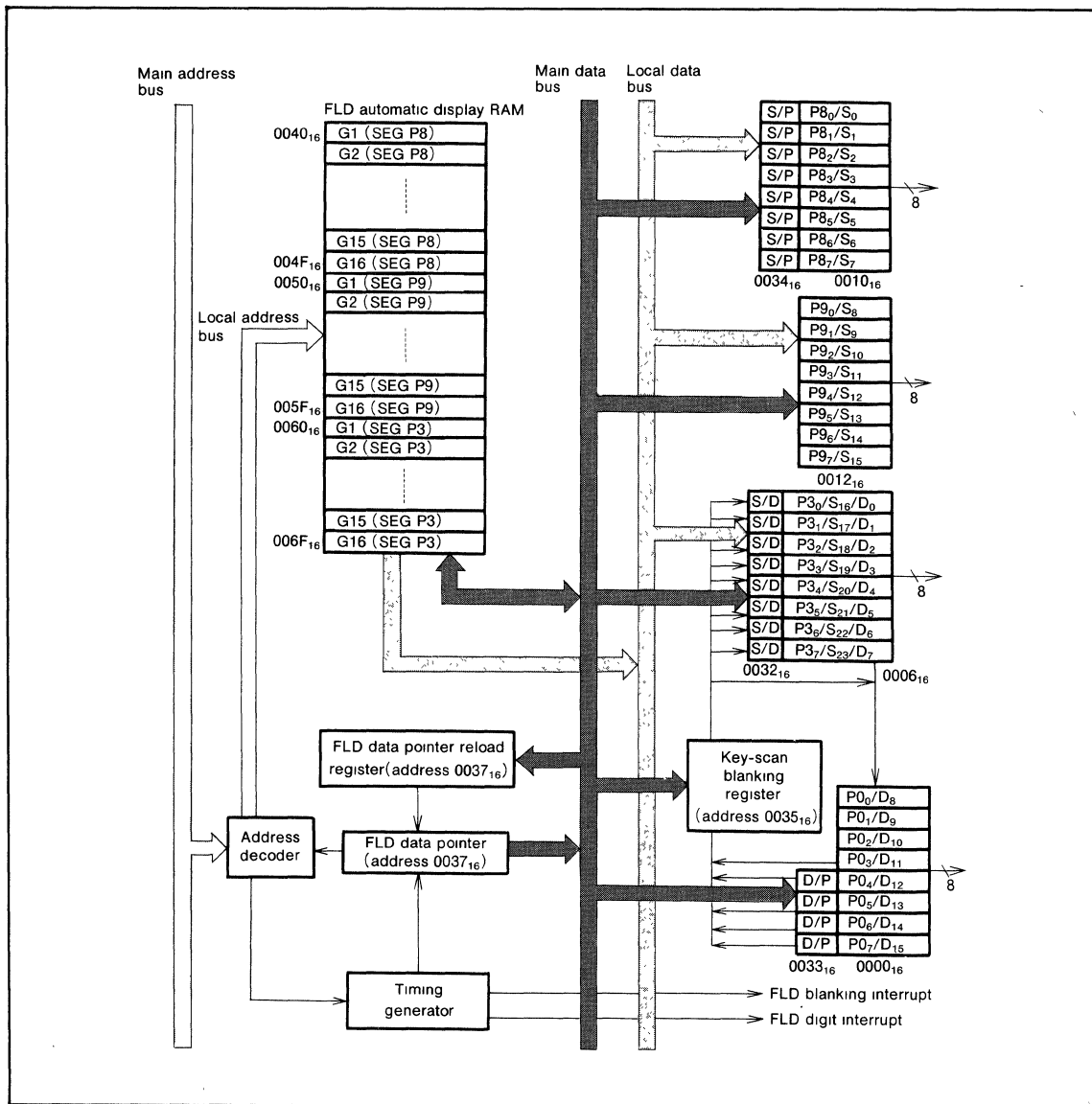


Fig. 27 FLD control circuit block diagram

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**FLDC Mode Register (FLDM)**

The FLDC mode register (address 0036<sub>16</sub>) is a seven bit control register which is used to control the FLD automatic display.

**Key-scan Blanking Register (KSCN)**

The key-scan blanking register (address 0035<sub>16</sub>) is a two bit register which sets the blanking period  $T_{scan}$  between the last digit and the first digit of the next cycle.

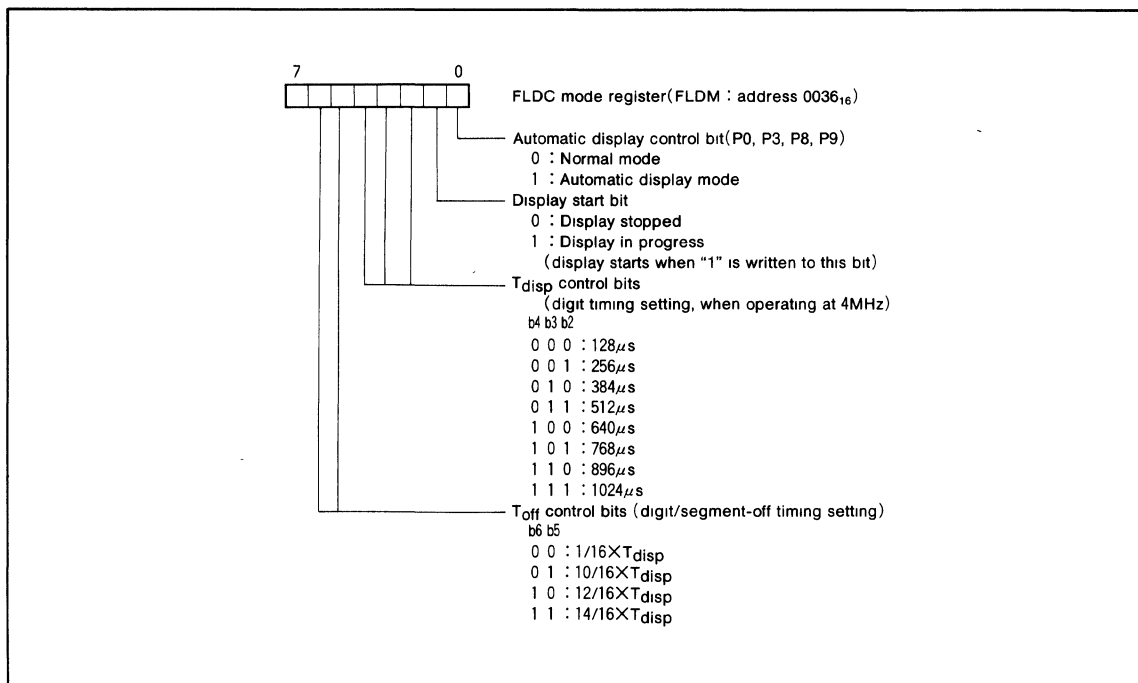


Fig. 28 Structure of FLDC mode register (FLDM)

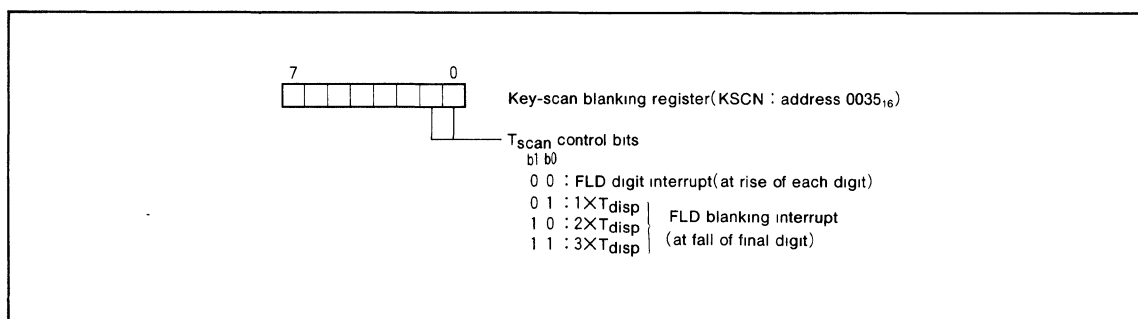


Fig. 29 Structure of key-scan blanking register (KSCN)

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**FLD Automatic Display Pins**

The FLD automatic display function of Ports P3, P0, P9, and P8 is selected by setting the automatic display control bit of

the FLDC mode register (address 0036<sub>16</sub>) to "1".

When using the FLD automatic display mode, set the number of segments and digits for each port.

**Table 5. Pins in FLD automatic display mode**

Port Name	Automatic Display Pins	Setting Method
P8 <sub>0</sub> -P8 <sub>7</sub>	SEG <sub>0</sub> -SEG <sub>7</sub> or P8 <sub>0</sub> -P8 <sub>7</sub>	The individual bits of the segment/port switching register (address 0034 <sub>16</sub> ) can be used to set each pin to either segment ("1") or normal port input ("0")
P9 <sub>0</sub> -P9 <sub>7</sub>	SEG <sub>8</sub> -SEG <sub>15</sub>	None (segment only)
P3 <sub>0</sub> -P3 <sub>7</sub>	SEG <sub>16</sub> -SEG <sub>23</sub> or DIG <sub>0</sub> -DIG <sub>7</sub>	The individual bits of the segment/digit switching register (address 0032 <sub>16</sub> ) can be used to set each pin to segment ("1") or digit ("0") (Note)
P0 <sub>0</sub> -P0 <sub>3</sub>	DIG <sub>8</sub> -DIG <sub>11</sub>	None (digit only)
P0 <sub>4</sub> -P0 <sub>7</sub>	DIG <sub>12</sub> -DIG <sub>15</sub> or P0 <sub>4</sub> -P0 <sub>7</sub>	The individual bits of the digit/port switching register (address 0033 <sub>16</sub> ) can be used to set each pin to digit ("1") or normal port output ("0") (Note)

Note. Always set digits in sequence

Number of segments Number of digits	16 4	8 12	16 10	24 8	16 16																																																																																
Port P8 (has segment/port switching register)	<table border="1"> <tr><td>0</td><td>P8<sub>0</sub></td></tr> <tr><td>0</td><td>P8<sub>1</sub></td></tr> <tr><td>0</td><td>P8<sub>2</sub></td></tr> <tr><td>0</td><td>P8<sub>3</sub></td></tr> <tr><td>0</td><td>P8<sub>4</sub></td></tr> <tr><td>0</td><td>P8<sub>5</sub></td></tr> <tr><td>0</td><td>P8<sub>6</sub></td></tr> <tr><td>0</td><td>P8<sub>7</sub></td></tr> </table>	0	P8 <sub>0</sub>	0	P8 <sub>1</sub>	0	P8 <sub>2</sub>	0	P8 <sub>3</sub>	0	P8 <sub>4</sub>	0	P8 <sub>5</sub>	0	P8 <sub>6</sub>	0	P8 <sub>7</sub>	<table border="1"> <tr><td>0</td><td>P8<sub>0</sub></td></tr> <tr><td>0</td><td>P8<sub>1</sub></td></tr> <tr><td>0</td><td>P8<sub>2</sub></td></tr> <tr><td>0</td><td>P8<sub>3</sub></td></tr> <tr><td>0</td><td>P8<sub>4</sub></td></tr> <tr><td>0</td><td>P8<sub>5</sub></td></tr> <tr><td>0</td><td>P8<sub>6</sub></td></tr> <tr><td>0</td><td>P8<sub>7</sub></td></tr> </table>	0	P8 <sub>0</sub>	0	P8 <sub>1</sub>	0	P8 <sub>2</sub>	0	P8 <sub>3</sub>	0	P8 <sub>4</sub>	0	P8 <sub>5</sub>	0	P8 <sub>6</sub>	0	P8 <sub>7</sub>	<table border="1"> <tr><td>0</td><td>P8<sub>0</sub></td></tr> <tr><td>0</td><td>P8<sub>1</sub></td></tr> <tr><td>0</td><td>P8<sub>2</sub></td></tr> <tr><td>0</td><td>P8<sub>3</sub></td></tr> <tr><td>1</td><td>SEG<sub>4</sub></td></tr> <tr><td>1</td><td>SEG<sub>5</sub></td></tr> <tr><td>1</td><td>SEG<sub>6</sub></td></tr> <tr><td>1</td><td>SEG<sub>7</sub></td></tr> </table>	0	P8 <sub>0</sub>	0	P8 <sub>1</sub>	0	P8 <sub>2</sub>	0	P8 <sub>3</sub>	1	SEG <sub>4</sub>	1	SEG <sub>5</sub>	1	SEG <sub>6</sub>	1	SEG <sub>7</sub>	<table border="1"> <tr><td>1</td><td>SEG<sub>0</sub></td></tr> <tr><td>1</td><td>SEG<sub>1</sub></td></tr> <tr><td>1</td><td>SEG<sub>2</sub></td></tr> <tr><td>1</td><td>SEG<sub>3</sub></td></tr> <tr><td>1</td><td>SEG<sub>4</sub></td></tr> <tr><td>1</td><td>SEG<sub>5</sub></td></tr> <tr><td>1</td><td>SEG<sub>6</sub></td></tr> <tr><td>1</td><td>SEG<sub>7</sub></td></tr> </table>	1	SEG <sub>0</sub>	1	SEG <sub>1</sub>	1	SEG <sub>2</sub>	1	SEG <sub>3</sub>	1	SEG <sub>4</sub>	1	SEG <sub>5</sub>	1	SEG <sub>6</sub>	1	SEG <sub>7</sub>	<table border="1"> <tr><td>1</td><td>SEG<sub>0</sub></td></tr> <tr><td>1</td><td>SEG<sub>1</sub></td></tr> <tr><td>1</td><td>SEG<sub>2</sub></td></tr> <tr><td>1</td><td>SEG<sub>3</sub></td></tr> <tr><td>1</td><td>SEG<sub>4</sub></td></tr> <tr><td>1</td><td>SEG<sub>5</sub></td></tr> <tr><td>1</td><td>SEG<sub>6</sub></td></tr> <tr><td>1</td><td>SEG<sub>7</sub></td></tr> </table>	1	SEG <sub>0</sub>	1	SEG <sub>1</sub>	1	SEG <sub>2</sub>	1	SEG <sub>3</sub>	1	SEG <sub>4</sub>	1	SEG <sub>5</sub>	1	SEG <sub>6</sub>	1	SEG <sub>7</sub>
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Port P9 (segment only)	<table border="1"> <tr><td>SEG<sub>8</sub></td></tr> <tr><td>SEG<sub>9</sub></td></tr> <tr><td>SEG<sub>10</sub></td></tr> <tr><td>SEG<sub>11</sub></td></tr> <tr><td>SEG<sub>12</sub></td></tr> <tr><td>SEG<sub>13</sub></td></tr> <tr><td>SEG<sub>14</sub></td></tr> <tr><td>SEG<sub>15</sub></td></tr> </table>	SEG <sub>8</sub>	SEG <sub>9</sub>	SEG <sub>10</sub>	SEG <sub>11</sub>	SEG <sub>12</sub>	SEG <sub>13</sub>	SEG <sub>14</sub>	SEG <sub>15</sub>	<table border="1"> <tr><td>SEG<sub>8</sub></td></tr> <tr><td>SEG<sub>9</sub></td></tr> <tr><td>SEG<sub>10</sub></td></tr> <tr><td>SEG<sub>11</sub></td></tr> <tr><td>SEG<sub>12</sub></td></tr> <tr><td>SEG<sub>13</sub></td></tr> <tr><td>SEG<sub>14</sub></td></tr> <tr><td>SEG<sub>15</sub></td></tr> </table>	SEG <sub>8</sub>	SEG <sub>9</sub>	SEG <sub>10</sub>	SEG <sub>11</sub>	SEG <sub>12</sub>	SEG <sub>13</sub>	SEG <sub>14</sub>	SEG <sub>15</sub>	<table border="1"> <tr><td>SEG<sub>8</sub></td></tr> <tr><td>SEG<sub>9</sub></td></tr> <tr><td>SEG<sub>10</sub></td></tr> <tr><td>SEG<sub>11</sub></td></tr> <tr><td>SEG<sub>12</sub></td></tr> <tr><td>SEG<sub>13</sub></td></tr> <tr><td>SEG<sub>14</sub></td></tr> <tr><td>SEG<sub>15</sub></td></tr> </table>	SEG <sub>8</sub>	SEG <sub>9</sub>	SEG <sub>10</sub>	SEG <sub>11</sub>	SEG <sub>12</sub>	SEG <sub>13</sub>	SEG <sub>14</sub>	SEG <sub>15</sub>	<table border="1"> <tr><td>SEG<sub>8</sub></td></tr> <tr><td>SEG<sub>9</sub></td></tr> <tr><td>SEG<sub>10</sub></td></tr> <tr><td>SEG<sub>11</sub></td></tr> <tr><td>SEG<sub>12</sub></td></tr> <tr><td>SEG<sub>13</sub></td></tr> <tr><td>SEG<sub>14</sub></td></tr> <tr><td>SEG<sub>15</sub></td></tr> </table>	SEG <sub>8</sub>	SEG <sub>9</sub>	SEG <sub>10</sub>	SEG <sub>11</sub>	SEG <sub>12</sub>	SEG <sub>13</sub>	SEG <sub>14</sub>	SEG <sub>15</sub>	<table border="1"> <tr><td>SEG<sub>8</sub></td></tr> <tr><td>SEG<sub>9</sub></td></tr> <tr><td>SEG<sub>10</sub></td></tr> <tr><td>SEG<sub>11</sub></td></tr> <tr><td>SEG<sub>12</sub></td></tr> <tr><td>SEG<sub>13</sub></td></tr> <tr><td>SEG<sub>14</sub></td></tr> <tr><td>SEG<sub>15</sub></td></tr> </table>	SEG <sub>8</sub>	SEG <sub>9</sub>	SEG <sub>10</sub>	SEG <sub>11</sub>	SEG <sub>12</sub>	SEG <sub>13</sub>	SEG <sub>14</sub>	SEG <sub>15</sub>																																								
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Port P0 (has digit/port switching register)	<table border="1"> <tr><td>DIG<sub>8</sub> → G4</td></tr> <tr><td>DIG<sub>9</sub> → G3</td></tr> <tr><td>DIG<sub>10</sub> → G2</td></tr> <tr><td>DIG<sub>11</sub> → G1</td></tr> <tr><td>0</td><td>P0<sub>4</sub></td></tr> <tr><td>0</td><td>P0<sub>5</sub></td></tr> <tr><td>0</td><td>P0<sub>6</sub></td></tr> <tr><td>0</td><td>P0<sub>7</sub></td></tr> </table>	DIG <sub>8</sub> → G4	DIG <sub>9</sub> → G3	DIG <sub>10</sub> → G2	DIG <sub>11</sub> → G1	0	P0 <sub>4</sub>	0	P0 <sub>5</sub>	0	P0 <sub>6</sub>	0	P0 <sub>7</sub>	<table border="1"> <tr><td>DIG<sub>8</sub> → G4</td></tr> <tr><td>DIG<sub>9</sub> → G3</td></tr> <tr><td>DIG<sub>10</sub> → G2</td></tr> <tr><td>DIG<sub>11</sub> → G1</td></tr> <tr><td>0</td><td>P0<sub>4</sub></td></tr> <tr><td>0</td><td>P0<sub>5</sub></td></tr> <tr><td>0</td><td>P0<sub>6</sub></td></tr> <tr><td>0</td><td>P0<sub>7</sub></td></tr> </table>	DIG <sub>8</sub> → G4	DIG <sub>9</sub> → G3	DIG <sub>10</sub> → G2	DIG <sub>11</sub> → G1	0	P0 <sub>4</sub>	0	P0 <sub>5</sub>	0	P0 <sub>6</sub>	0	P0 <sub>7</sub>	<table border="1"> <tr><td>DIG<sub>8</sub> → G6</td></tr> <tr><td>DIG<sub>9</sub> → G5</td></tr> <tr><td>DIG<sub>10</sub> → G4</td></tr> <tr><td>DIG<sub>11</sub> → G3</td></tr> <tr><td>1</td><td>DIG<sub>12</sub> → G2</td></tr> <tr><td>1</td><td>DIG<sub>13</sub> → G1</td></tr> <tr><td>0</td><td>P0<sub>6</sub></td></tr> <tr><td>0</td><td>P0<sub>7</sub></td></tr> </table>	DIG <sub>8</sub> → G6	DIG <sub>9</sub> → G5	DIG <sub>10</sub> → G4	DIG <sub>11</sub> → G3	1	DIG <sub>12</sub> → G2	1	DIG <sub>13</sub> → G1	0	P0 <sub>6</sub>	0	P0 <sub>7</sub>	<table border="1"> <tr><td>DIG<sub>8</sub> → G8</td></tr> <tr><td>DIG<sub>9</sub> → G7</td></tr> <tr><td>DIG<sub>10</sub> → G6</td></tr> <tr><td>DIG<sub>11</sub> → G5</td></tr> <tr><td>1</td><td>DIG<sub>12</sub> → G4</td></tr> <tr><td>1</td><td>DIG<sub>13</sub> → G3</td></tr> <tr><td>1</td><td>DIG<sub>14</sub> → G2</td></tr> <tr><td>1</td><td>DIG<sub>15</sub> → G1</td></tr> </table>	DIG <sub>8</sub> → G8	DIG <sub>9</sub> → G7	DIG <sub>10</sub> → G6	DIG <sub>11</sub> → G5	1	DIG <sub>12</sub> → G4	1	DIG <sub>13</sub> → G3	1	DIG <sub>14</sub> → G2	1	DIG <sub>15</sub> → G1	<table border="1"> <tr><td>DIG<sub>8</sub> → G8</td></tr> <tr><td>DIG<sub>9</sub> → G7</td></tr> <tr><td>DIG<sub>10</sub> → G6</td></tr> <tr><td>DIG<sub>11</sub> → G5</td></tr> <tr><td>1</td><td>DIG<sub>12</sub> → G4</td></tr> <tr><td>1</td><td>DIG<sub>13</sub> → G3</td></tr> <tr><td>1</td><td>DIG<sub>14</sub> → G2</td></tr> <tr><td>1</td><td>DIG<sub>15</sub> → G1</td></tr> </table>	DIG <sub>8</sub> → G8	DIG <sub>9</sub> → G7	DIG <sub>10</sub> → G6	DIG <sub>11</sub> → G5	1	DIG <sub>12</sub> → G4	1	DIG <sub>13</sub> → G3	1	DIG <sub>14</sub> → G2	1	DIG <sub>15</sub> → G1																				
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1	DIG <sub>15</sub> → G1																																																																																				

**Fig. 30 Segment/digit setting example**



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**FLD Automatic Display RAM**

The FLD automatic display RAM area is the 48 bytes from addresses 0040<sub>16</sub> to 006F<sub>16</sub>. The FLD automatic display RAM area can be used to store 3-byte data items for a maximum of 16 digits. Addresses 0040<sub>16</sub> to 004F<sub>16</sub> are used for P8 segment data, addresses 0050<sub>16</sub> to 005F<sub>16</sub> are used for P9 segment data, and addresses 0060<sub>16</sub> to 006F<sub>16</sub> are used for P3 segment data.

- **FLD Data Pointer and FLD Data Pointer Reload Register**  
 The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment, and the FLD data pointer reload register indicates the address of the first digit of segment P9.

Both the FLD data pointer and the FLD data pointer reload register are allocated to address 0037<sub>16</sub> and are 6-bits wide. Data written to this address is written to the FLD data pointer reload register, data read from this address is read from the FLD data pointer.

The actual memory address is the value of the data pointer plus 40<sub>16</sub>, 50<sub>16</sub>, or 60<sub>16</sub>.

The contents of the FLD data pointer indicate the start address of segment P9 at the start of automatic display. If segment P3 or P9 data is transferred to the segment, the FLD data pointer returns - 16; if segment P8 data is transferred, it returns + 31. After it reaches "00", the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, three bytes of data for the P3, P9, and P8 segments of one digit are transferred.

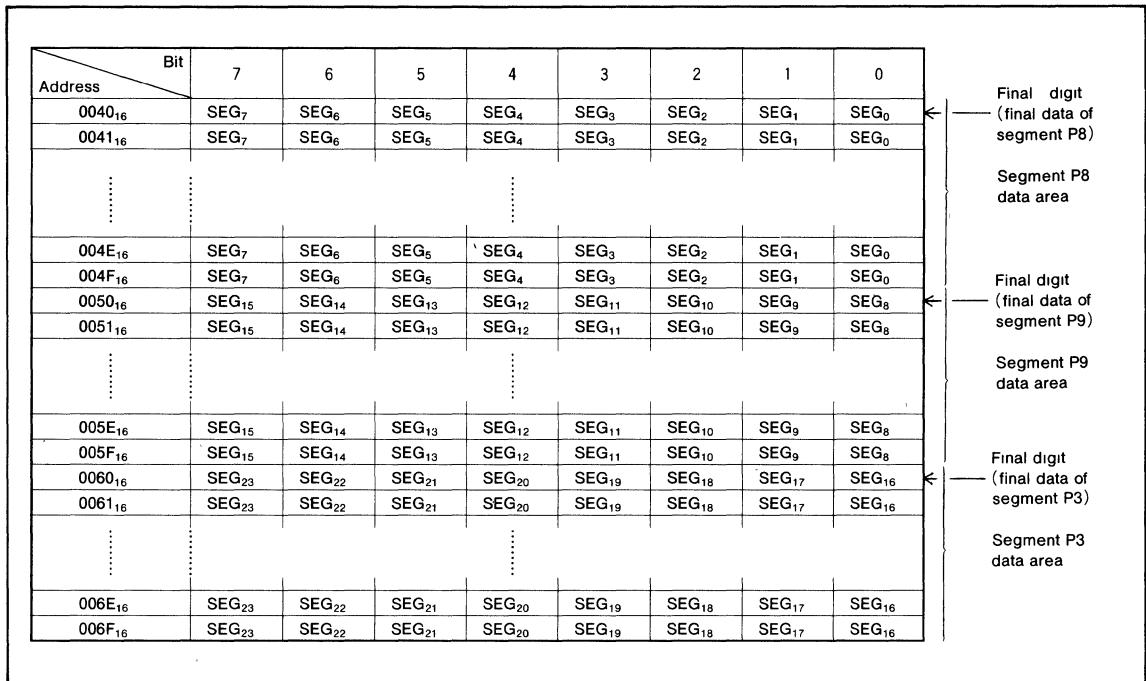


Fig. 31 FLD automatic display RAM and bit allocation

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• Data Setup

When data is stored in the FLD automatic display RAM, the end of segment P8 data is stored at address 0040<sub>16</sub>, the end of segment P9 data is stored at address 0050<sub>16</sub>, and the end of segment P3 data is stored at address 0060<sub>16</sub>. The head of each of the segment P8, P9, and P3 data is stored at an address that is the number of digits—1 away from the corresponding address 0040<sub>16</sub>, 0050<sub>16</sub>, 0060<sub>16</sub>.

Set the FLD data pointer reload register to the value given by the number of digits—1. "1" is always written to bit 5, and "0" is always written to bit 4. Note that "0" is always read from bit 5 or 4 during a read.

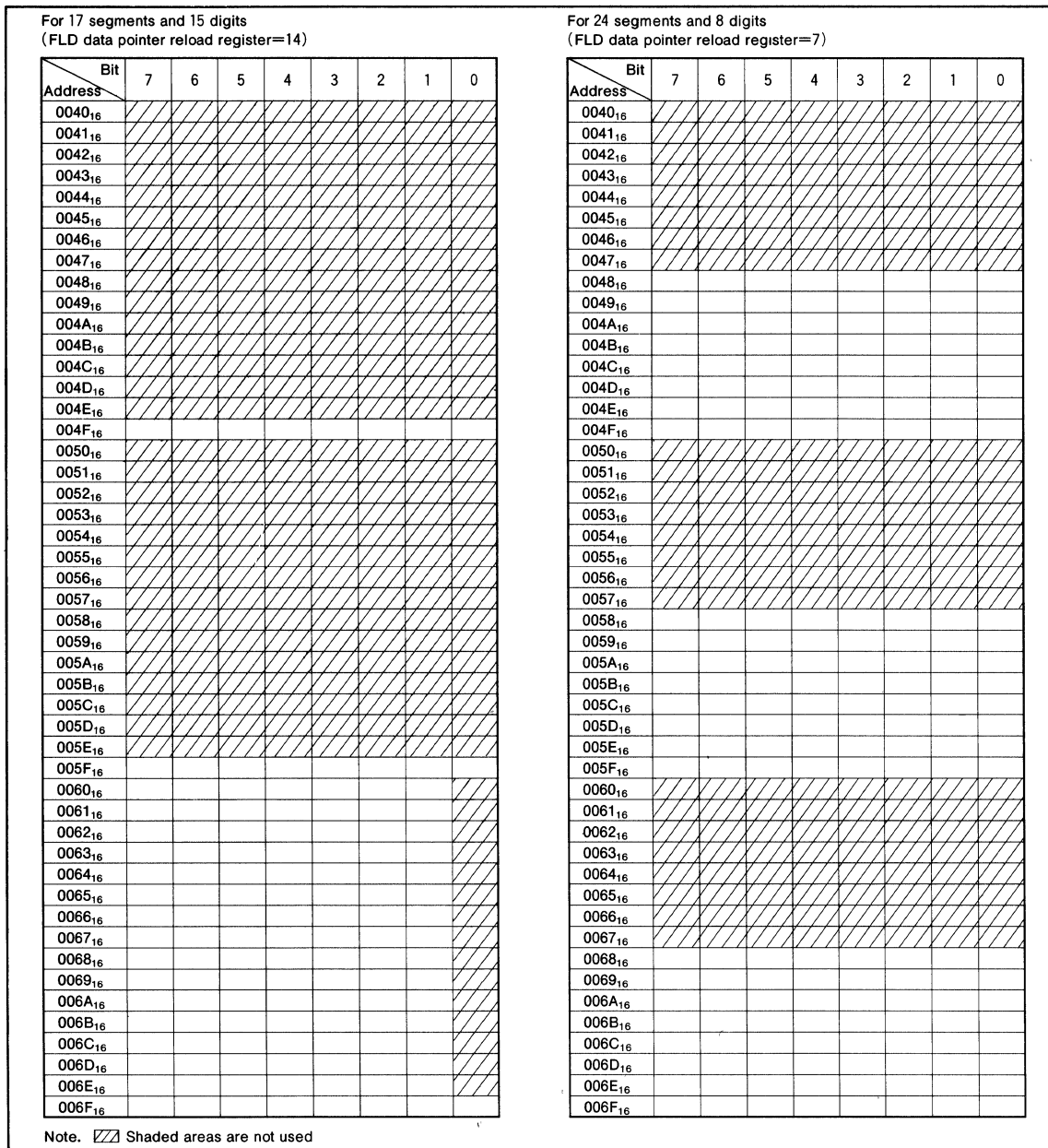


Fig. 32 Example of using the FLD automatic display RAM.

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• Timing Setting

The digit timing ( $T_{disp}$ ) and digit/segment turn-off timing ( $T_{off}$ ) can be set by the FLDC mode register (address  $0036_{16}$ ). The scan timing ( $T_{scan}$ ) can be set by the key-scan blanking register (address  $0035_{16}$ ).

Note that flickering will occur if the repetition frequency ( $1/(T_{disp} \times \text{number of digits} + T_{scan})$ ) is an integral multiple of the digit timing  $T_{disp}$ .

• FLD Start

To perform FLD automatic display, you have to use the following registers.

- Port P3 segment/digit switching register
- Port P0 digit/port switching register
- Port P8 segment/port switching register
- Key-scan blanking register
- FLDC mode register
- FLD data pointer

Automatic display mode is activated by writing "1" to bit 0

of the FLDC mode register (address  $0036_{16}$ ), and the automatic display is started by writing "1" to bit 1. During automatic display bit 1 always keeps "1", automatic display can be interrupted by writing "0" to bit 1.

If key-scan is to be performed by segment during the key-scan blanking period  $T_{scan}$ ,

1. Write "0" to bit 0 (automatic display control bit) of FLDC mode register (address  $0036_{16}$ ).
2. Set the port corresponding to the segment to the normal port.
3. After the key-scan is performed, write "1" (automatic display mode) to bit 0 of FLDC mode register (address  $0036_{16}$ ).

Note on performance of key-scan in the above 1 to 3 order.

1. Do not write "0" to bit 1 of FLDC mode register (address  $0036_{16}$ ).
2. Do not write "1" to the port corresponding to the digit.

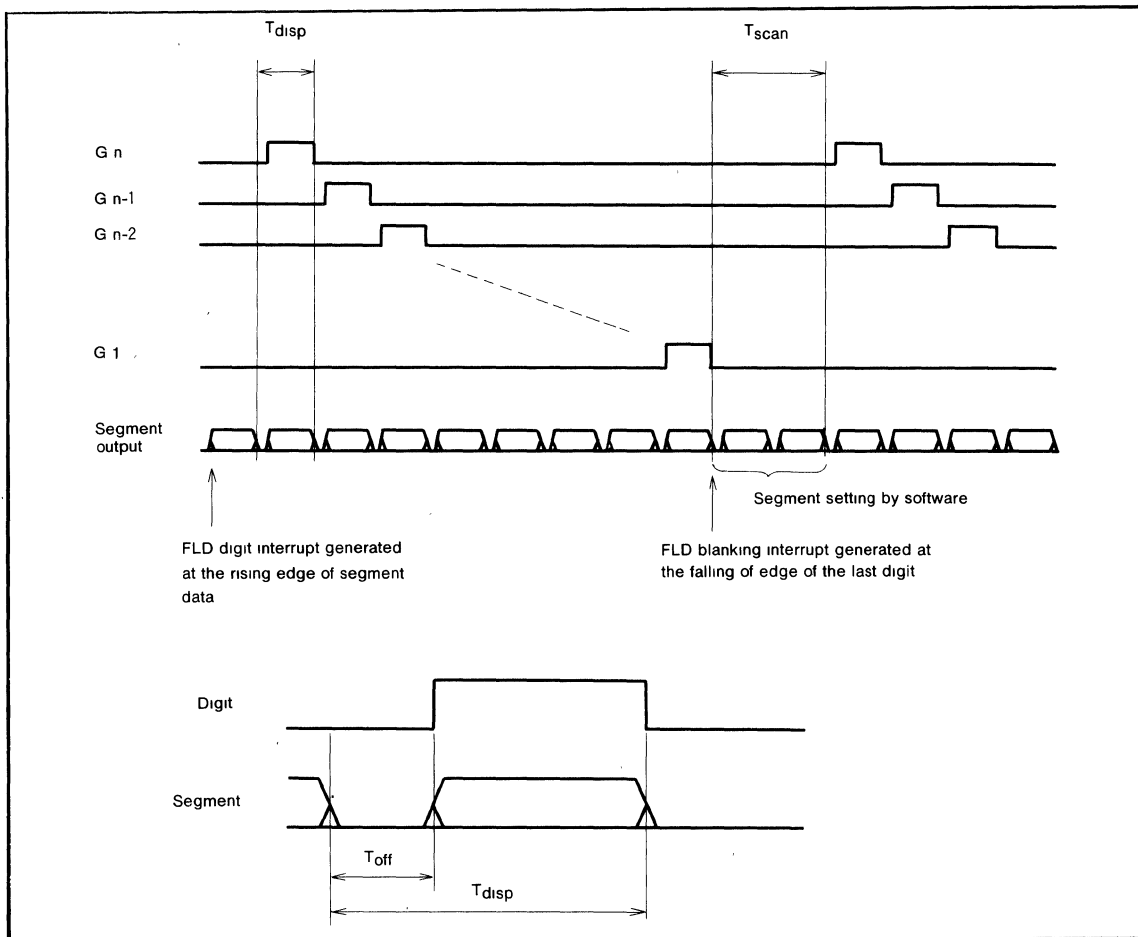


Fig. 33 FLDC timing

## SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## RESET CIRCUIT

After a reset, the microcomputer will start in high-speed operation start mode or low-speed operation start mode depending on a mask-programmable option.

- High-Speed Operation Start Mode

In high-speed operation start mode, reset occurs if the  $\overline{\text{RESET}}$  pin is held at an "L" level for at least  $2\mu\text{s}$  then is returned to an "H" level (the power supply voltage should be between 4.0V and 5.5V). Both the  $X_{\text{IN}}$  and the  $X_{\text{CIN}}$  clocks begin oscillating. In order to give the  $X_{\text{IN}}$  clock time to stabilize, internal operation does not begin until after 13  $X_{\text{IN}}$  clock cycles are complete. After the reset is completed, the program starts from the address contained in address  $\text{FFFD}_{16}$  (upper byte) and address  $\text{FFFC}_{16}$  (lower byte).

- Low-Speed Operation Start Mode

In low-speed operation start mode, reset occurs if the  $\overline{\text{RESET}}$  pin is held at an "L" level for at least  $2\mu\text{s}$  then is

returned to an "H" level (the power supply voltage should be between 2.8V and 5.5V). The  $X_{\text{IN}}$  clock does not begin oscillating. In order to give the  $X_{\text{CIN}}$  time to stabilize, timer 1 and timer 2 are connected together and 512 cycles of the  $X_{\text{CIN}}/16$  are counted before internal operation begins. After the reset is completed, the program starts from the address contained in address  $\text{FFFD}_{16}$  (upper byte) and address  $\text{FFFC}_{16}$  (lower byte).

If the  $X_{\text{CIN}}$  clock is stable, reset will complete after approximately 250ms (assuming  $f(X_{\text{CIN}})=32.768\text{kHz}$ ).

Immediately after a power-on, the stability of the clock circuit will determine the reset timing and will vary according to the characteristics of the oscillation circuit used.

- Note on Use

Make sure that the reset input voltage is no more than 0.8V in high-speed operation start mode, or no more than 0.5V in low-speed operation start mode.

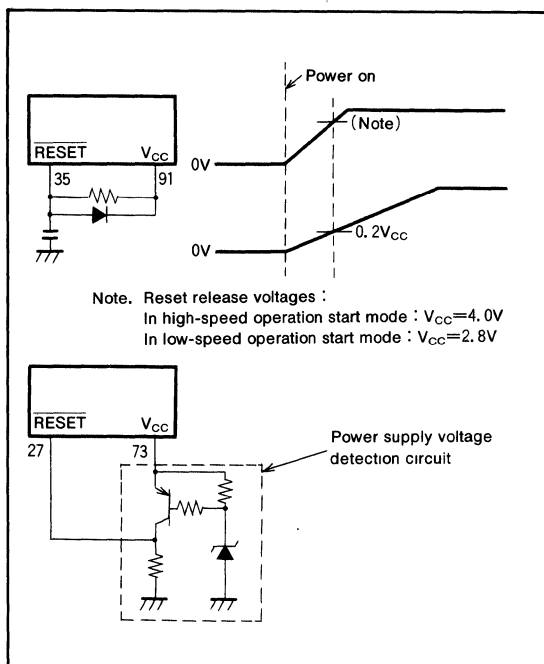


Fig. 34 Power-on reset circuit example

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	Address	Register contents		Address	Register contents
(1) Port P0 register	(0 0 0 0 <sub>16</sub> )...	00 <sub>16</sub>	(31) Timer 12 mode register	(0 0 2 8 <sub>16</sub> )...	00 <sub>16</sub>
(2) Port P1 register	(0 0 0 2 <sub>16</sub> )...	00 <sub>16</sub>	(32) Timer 34 mode register	(0 0 2 9 <sub>16</sub> )...	00 <sub>16</sub>
(3) Port P1 direction register	(0 0 0 3 <sub>16</sub> )...	00 <sub>16</sub>	(33) Timer 56 mode register	(0 0 2 A <sub>16</sub> )...	00 <sub>16</sub>
(4) Port P2 register	(0 0 0 4 <sub>16</sub> )...	00 <sub>16</sub>	(34) PWM control register	(0 0 2 B <sub>16</sub> )...	00 <sub>16</sub>
(5) Port P2 direction register	(0 0 0 5 <sub>16</sub> )...	00 <sub>16</sub>	(35) A-D control register	(0 0 3 0 <sub>16</sub> )...	08 <sub>16</sub>
(6) Port P3 register	(0 0 0 6 <sub>16</sub> )...	00 <sub>16</sub>	(36) Port P3 segment/digit switching register	(0 0 3 2 <sub>16</sub> )...	00 <sub>16</sub>
(7) Port P4 register	(0 0 0 8 <sub>16</sub> )...	00 <sub>16</sub>	(37) Port P0 digit/port switching register	(0 0 3 3 <sub>16</sub> )...	00 <sub>16</sub>
(8) Port P4 direction register	(0 0 0 9 <sub>16</sub> )...	00 <sub>16</sub>	(38) Port P8 segment/port switching register	(0 0 3 4 <sub>16</sub> )...	00 <sub>16</sub>
(9) Port P5 register	(0 0 0 A <sub>16</sub> )...	00 <sub>16</sub>	(39) Key-scan blanking register	(0 0 3 5 <sub>16</sub> )...	00 <sub>16</sub>
(10) Port P5 direction register	(0 0 0 B <sub>16</sub> )...	00 <sub>16</sub>	(40) FLDC mode register	(0 0 3 6 <sub>16</sub> )...	00 <sub>16</sub>
(11) Port P6 register	(0 0 0 C <sub>16</sub> )...	00 <sub>16</sub>	(41) High-breakdown-voltage port control register	(0 0 3 8 <sub>16</sub> )...	00 <sub>16</sub>
(12) Port P6 direction register	(0 0 0 D <sub>16</sub> )...	00 <sub>16</sub>	(42) Interrupt edge selection register	(0 0 3 A <sub>16</sub> )...	00 <sub>16</sub>
(13) Port P7 register	(0 0 0 E <sub>16</sub> )...	00 <sub>16</sub>	(43) CPU mode register	(0 0 3 B <sub>16</sub> )...	* * 1 0 0 0 0 0
(14) Port P7 direction register	(0 0 0 F <sub>16</sub> )...	00 <sub>16</sub>	(44) Interrupt request register 1	(0 0 3 C <sub>16</sub> )...	00 <sub>16</sub>
(15) Port P8 register	(0 0 1 0 <sub>16</sub> )...	00 <sub>16</sub>	(45) Interrupt request register 2	(0 0 3 D <sub>16</sub> )...	00 <sub>16</sub>
(16) Port P8 direction register	(0 0 1 1 <sub>16</sub> )...	00 <sub>16</sub>	(46) Interrupt control register 1	(0 0 3 E <sub>16</sub> )...	00 <sub>16</sub>
(17) Port P9 register	(0 0 1 2 <sub>16</sub> )...	00 <sub>16</sub>	(47) Interrupt control register 2	(0 0 3 F <sub>16</sub> )...	00 <sub>16</sub>
(18) Port P9 direction register	(0 0 1 3 <sub>16</sub> )...	00 <sub>16</sub>	(48) Processor status register	(P S) <sub>4</sub>	× × × × 1 × ×
(19) Port PA register	(0 0 1 4 <sub>16</sub> )...	00 <sub>16</sub>	(49) Program counter	(P C <sub>H</sub> )	Contents of address FFFD <sub>16</sub>
(20) Port PA direction register	(0 0 1 5 <sub>16</sub> )...	00 <sub>16</sub>		(P C <sub>L</sub> )	Contents of address FFFC <sub>16</sub>
(21) Serial I/O1 control register	(0 0 1 9 <sub>16</sub> )...	00 <sub>16</sub>			
(22) Serial I/O automatic transfer control register	(0 0 1 A <sub>16</sub> )...	00 <sub>16</sub>			
(23) Serial I/O automatic transfer interval register	(0 0 1 C <sub>16</sub> )...	00 <sub>16</sub>			
(24) Serial I/O2 control register	(0 0 1 D <sub>16</sub> )...	00 <sub>16</sub>			
(25) Timer 1 register	(0 0 2 0 <sub>16</sub> )...	FF <sub>16</sub>			
(26) Timer 2 register	(0 0 2 1 <sub>16</sub> )...	01 <sub>16</sub>			
(27) Timer 3 register	(0 0 2 2 <sub>16</sub> )...	FF <sub>16</sub>			
(28) Timer 4 register	(0 0 2 3 <sub>16</sub> )...	FF <sub>16</sub>			
(29) Timer 5 register	(0 0 2 4 <sub>16</sub> )...	FF <sub>16</sub>			
(30) Timer 6 register	(0 0 2 5 <sub>16</sub> )...	FF <sub>16</sub>			

Note. \* : The initial values of bits 7 and 6 of the CPU mode register are determined by a mask option  
 × : Undefined  
 The contents of all other registers and RAM are undefined after a reset, so programs must set their initial values

Fig. 35 Internal status at reset

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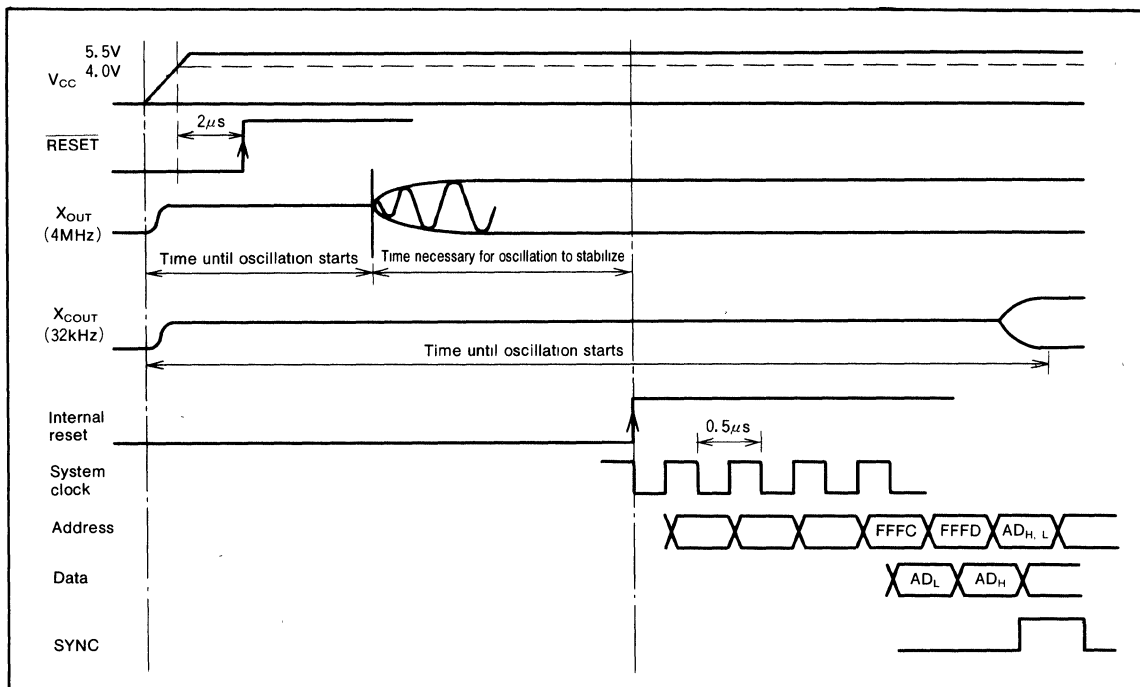


Fig. 36 Reset sequence in high-speed operation mode

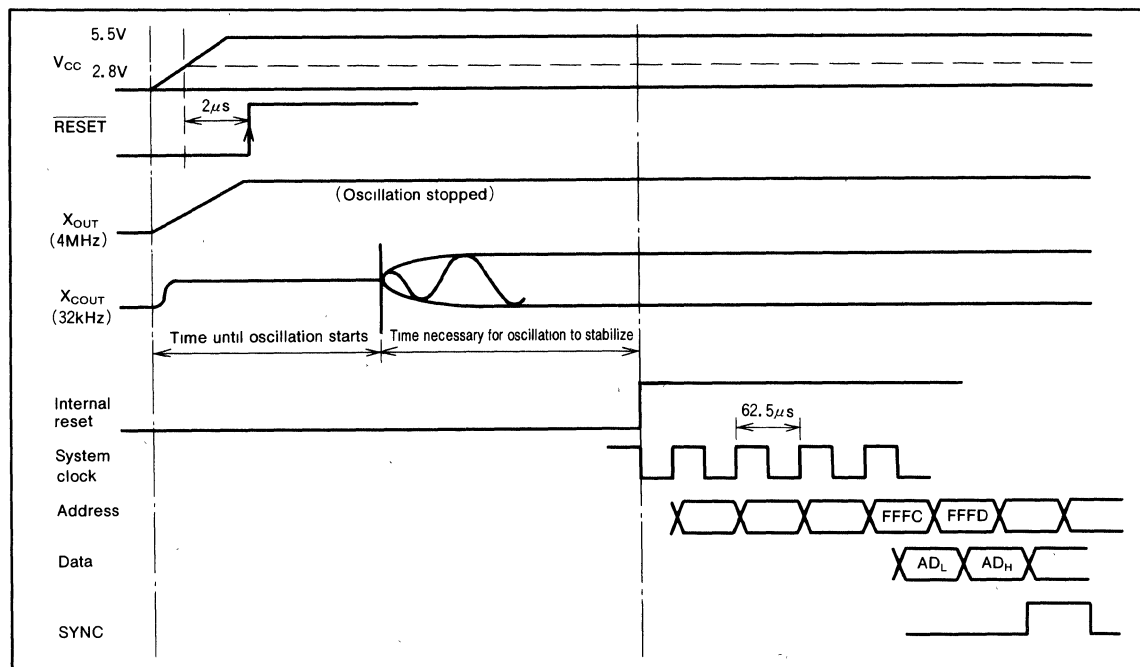


Fig. 37 Reset sequence in low-speed operation mode

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**CLOCK GENERATION CIRCUIT**

When using an external clock signal, input the clock signal to the  $X_{IN}$  ( $X_{CIN}$ ) pin and leave the  $X_{OUT}$  ( $X_{COUT}$ ) pin open. If the  $X_{CIN}$  clock is not used, connect the  $X_{CIN}$  pin to  $V_{SS}$ , and leave the  $X_{COUT}$  pin open.

Either high-speed operation start mode or low-speed operation start mode can be selected by using a mask option.

• **High-Speed Operation Start Mode**

After reset has completed, the internal clock  $\phi$  is half the frequency of  $X_{IN}$ . Immediately after power-on, both the  $X_{IN}$  and  $X_{CIN}$  clock start oscillating. To set the internal clock  $\phi$  to low-speed operation mode, set bit 7 of the CPU mode register (address  $003B_{16}$ ) to "1".

• **Low-Speed Operation Start Mode**

After reset has completed, the internal clock  $\phi$  is half the frequency of  $X_{CIN}$ . Immediately after power-on, only the  $X_{CIN}$  clock starts oscillating. To set the internal clock  $\phi$  to high-speed operation mode, first set bit 6 ( $CM_6$ ) of the CPU mode register (address  $003B_{16}$ ) to "0", then set bit 7 ( $CM_7$ ) to "0". Note that the program must allow time for oscillation to stabilize.

• **Oscillation Control Stop Mode**

If the STP instruction is executed, oscillation stops with the internal clock  $\phi$  at an "H" level. Timer 1 is set to " $FF_{16}$ " and timer 2 is set to " $01_{16}$ ".

Either  $X_{IN}$  or  $X_{CIN}$  divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The timer 1 and timer 2 interrupt enable bits must be set to disabled ("0"), so a program must set these bits before executing an STP instruction. Oscillation restarts at reset or when an external interrupt is received, but the internal clock  $\phi$  is not supplied to the CPU until timer 2 overflows. This allows time for the clock circuit oscillation to stabilize.

**Wait Mode**

If the WIT instruction is executed, the internal clock  $\phi$  stops at an "H" level but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

**Low-Speed Mode**

If the internal clock is generated from the sub clock ( $X_{CIN}$ ), a low power consumption operation can be entered by stopping only the main clock  $X_{IN}$ . To stop the main clock, set bit 6 ( $CM_6$ ) of the CPU mode register ( $003B_{16}$ ) to "1". When the main clock  $X_{IN}$  is restarted, the program must allow enough time for oscillation to stabilize.

Note that in low-power-consumption mode the  $X_{CIN}$ - $X_{COUT}$  drive performance can be reduced, allowing even lower power consumption ( $20\mu A$  with  $X_{CIN} = 32kHz$ ). To reduce the  $X_{CIN}$ - $X_{COUT}$  drive performance, clear bit 5 ( $CM_5$ ) of the CPU mode register ( $003B_{16}$ ) to "0". At re-

set or when an STP instruction is executed, this bit is set to "1" and strong drive is selected to help the oscillation to start.

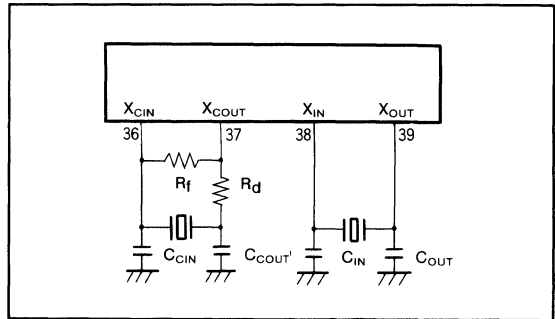


Fig. 38 Ceramic resonator circuit

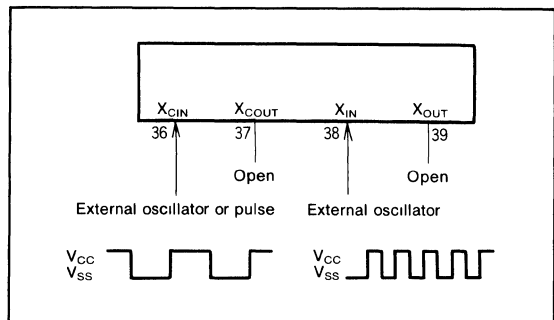


Fig. 39 External clock input circuit

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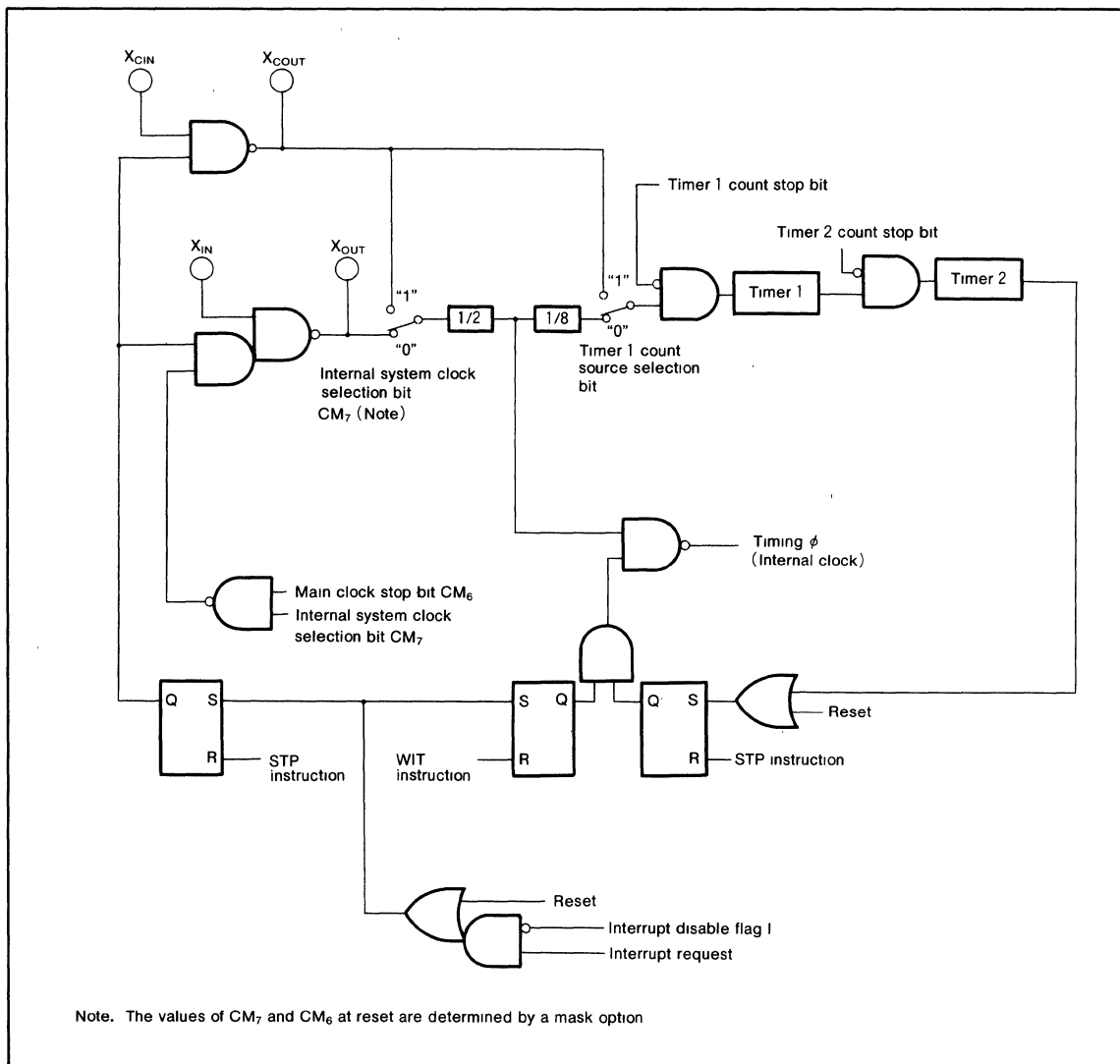


Fig. 40 System clock generation circuit block diagram



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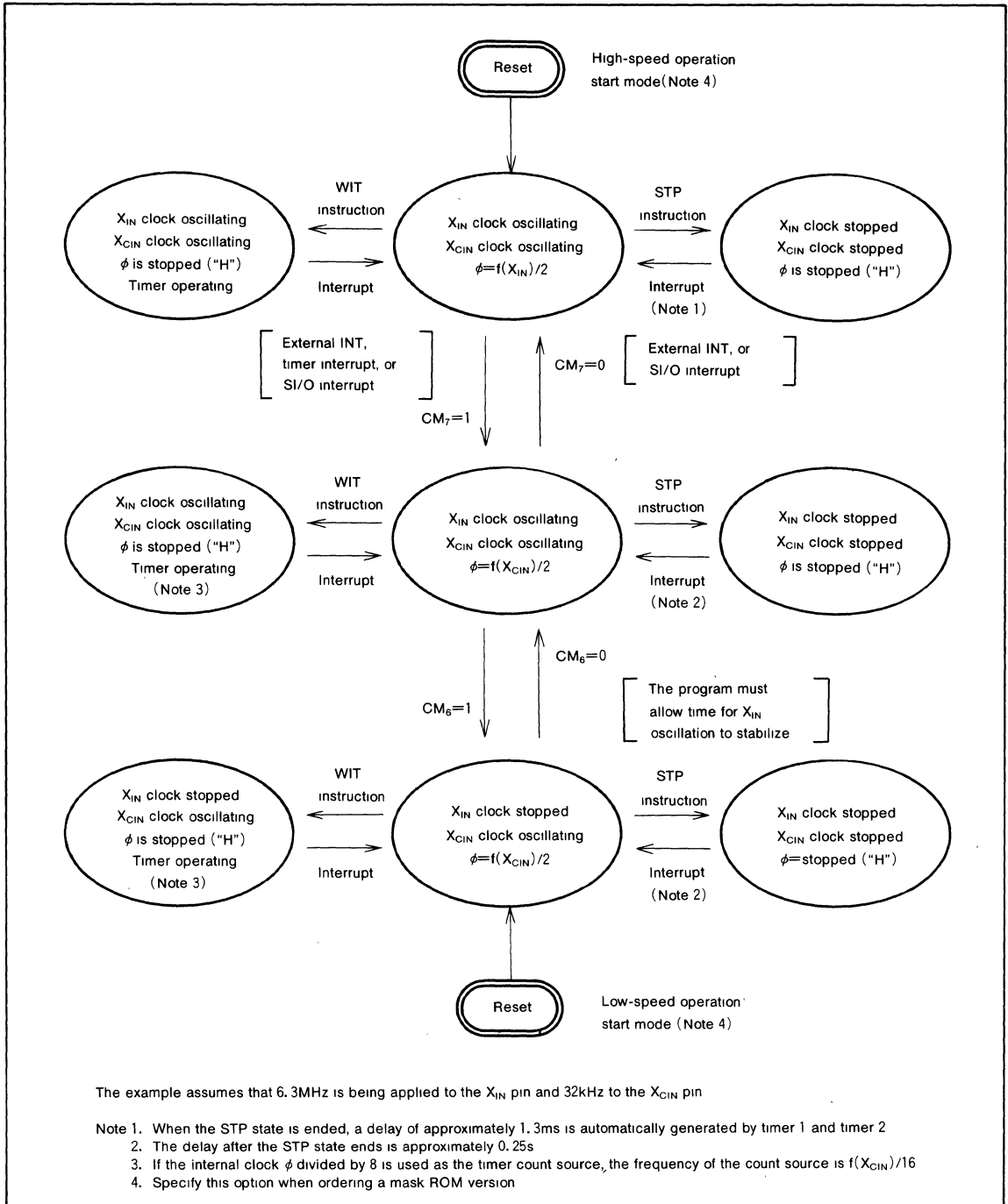


Fig. 41 State transitions of system clock

## NOTES ON PROGRAMMING

### • Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because of their effect on calculations.

### • Interrupts

The contents of the interrupt request bits do not change immediately after they have been written.

After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

### • Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

### • Timers

If a value  $n$  (between 0 and 255) is written to a timer latch, the frequency division ratio is  $1/(n+1)$ .

### • Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.

The execution of these instructions does not change the contents of the processor status register.

### • Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

### • Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing a serial I/O transfer.

When using the internal clock, set the synchronization clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer.

### • Instruction Execution Timing

The instruction execution time is obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction

is shown in the list of machine instructions.

The frequency of the internal clock  $\phi$  is half of the  $X_{IN}$  or  $X_{CIN}$  frequency.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**DATA REQUIRED FOR MASK ORDERS**

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form  
(three identical copies)

If required, specify the following option on the Mask Confirmation Form:

- Operation start mode switching option

**ROM Writing Method**

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

In case PROM is 32K bytes or under;

Package	Name of Write Adapter
100P6S	PCA4738F-100
100D0	PCA4738L-100

In case PROM is 36K bytes or over;

Package	Name of Write Adapter
100P6S	Under development
100D0	Under development

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 42 is recommended to verify programming.

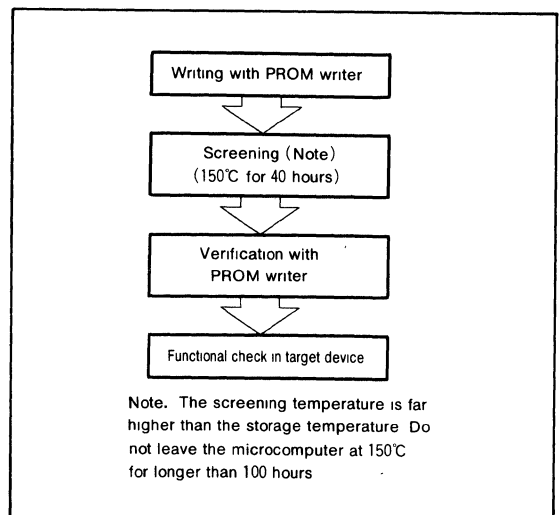


Fig. 42 Writing and testing of one-time programmable version

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	All voltages measured based on the V <sub>SS</sub> pin Output transistors are isolated	-0.3 to 7.0	V
V <sub>EE</sub>	Pull-down power supply voltage		V <sub>CC</sub> -40 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>3</sub> , PA <sub>0</sub> -PA <sub>7</sub> , PB <sub>0</sub> , PB <sub>1</sub>		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage P4 <sub>0</sub>		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage P8 <sub>0</sub> -P8 <sub>7</sub>		V <sub>CC</sub> -40 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage RESET, X <sub>IN</sub>		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage X <sub>CIN</sub>		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage P0 <sub>0</sub> -P0 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>		V <sub>CC</sub> -40 to V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub> , X <sub>OUT</sub> , X <sub>COU</sub> T		-0.3 to V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation		T <sub>a</sub> = 25°C	600
T <sub>opr</sub>	Operating temperature		-10 to 85	°C
T <sub>stg</sub>	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (V<sub>CC</sub> = 4.0 to 5.5V, T<sub>a</sub> = -10 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min	Typ	Max		
V <sub>CC</sub>	Supply voltage	High-speed operation mode	4.0	5.0	5.5	V
		Low-speed operation mode	2.8	5.0	5.5	
V <sub>SS</sub>	Supply voltage		0		V	
V <sub>EE</sub>	Pull-down power supply voltage	V <sub>CC</sub> -38		V <sub>CC</sub>	V	
V <sub>REF</sub>	Reference input voltage	2		V <sub>CC</sub>	V	
AV <sub>SS</sub>	Analog power voltage		0		V	
V <sub>IA</sub>	Analog input voltage	0		V <sub>CC</sub>	V	
V <sub>IH</sub>	"H" input voltage P1 <sub>0</sub> -P1 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub> , PB <sub>0</sub> , PB <sub>1</sub>	0.75V <sub>CC</sub>		V <sub>CC</sub>	V	
V <sub>IH</sub>	"H" input voltage P2 <sub>0</sub> -P2 <sub>7</sub>	0.4V <sub>CC</sub>		V <sub>CC</sub>	V	
V <sub>IH</sub>	"H" input voltage P4 <sub>0</sub>	0.75V <sub>CC</sub>		V <sub>CC</sub>	V	
V <sub>IH</sub>	"H" input voltage P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>3</sub>	0.8V <sub>CC</sub>		V <sub>CC</sub>	V	
V <sub>IH</sub>	"H" input voltage RESET	0.8V <sub>CC</sub>		V <sub>CC</sub>	V	
V <sub>IH</sub>	"H" input voltage X <sub>IN</sub> , X <sub>CIN</sub>	0.8V <sub>CC</sub>		V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage P1 <sub>0</sub> -P1 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub> , PB <sub>0</sub> , PB <sub>1</sub>	0		0.25V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage P2 <sub>0</sub> -P2 <sub>7</sub>	0		0.16V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage P4 <sub>0</sub>	0		0.25V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>3</sub>	0		0.2V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage RESET	0		0.2V <sub>CC</sub>	V	
V <sub>IL</sub>	"L" input voltage X <sub>IN</sub> , X <sub>CIN</sub>	0		0.2V <sub>CC</sub>	V	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

RECOMMENDED OPERATING CONDITIONS ( $V_{CC}=4.0$  to  $5.5V$ ,  $T_a=-10$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$\Sigma I_{OH(peak)}$	"H" total peak output current P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , (Note 1) P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>			-240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>5</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			-60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>1</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current P6 <sub>0</sub>			3.0	mA
$\Sigma I_{OH(avg)}$	"H" total average output current P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , (Note 1) P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>			-120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			-30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>1</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			50	mA
$\Sigma I_{OL(avg)}$	"L" total average output current P6 <sub>0</sub>			1.5	mA
$I_{OH(peak)}$	"H" peak output current P0 <sub>0</sub> -P0 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> (Note 2)			-40	mA
$I_{OH(peak)}$	"H" peak output current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			-10	mA
$I_{OL(peak)}$	"L" peak output current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>1</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			10	mA
$I_{OL(peak)}$	"L" peak output current P5 <sub>0</sub> -P5 <sub>7</sub>			10	mA
$I_{OL(peak)}$	"L" peak output current P6 <sub>0</sub>			3.0	mA
$I_{OH(avg)}$	"H" average output current P0 <sub>0</sub> -P0 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>			-18	mA
$I_{OH(avg)}$	"H" average output current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>1</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			-5.0	mA
$I_{OL(avg)}$	"L" average output current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , (Note 3) P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>			5.0	mA
$I_{OL(avg)}$	"L" average output current P5 <sub>0</sub> -P5 <sub>7</sub>			5.0	mA
$I_{OL(avg)}$	"L" average output current P6 <sub>0</sub>			1.5	mA
$f(CNTR_0)$	Clock input frequency for timers 2 and 4			250	kHz
$f(CNTR_1)$	(duty cycle 50%)				
$f(X_{IN})$	Main clock input oscillation frequency (Note 4)			6.3	MHz
$f(X_{CIN})$	Sub clock input oscillation frequency (Note 4, Note 5)		32.768	50	kHz

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents.

- The peak output current is the peak current flowing in each port.
- The average output current is an average value measured over 100ms.
- When the oscillation frequency has a duty cycle of 50%.
- When using the microcomputer in low-speed operation mode, make sure that the sub clock's input frequency  $f(X_{CIN})$  is less than  $f(X_{IN})/3$ .

# MITSUBISHI MICROCOMPUTERS

## M3818x Group

### SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

#### ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.0$ to $5.5V$ , $T_a = -10$ to $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
$V_{OH}$	"H" output voltage P0 <sub>0</sub> -P0 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>	$I_{OH} = -18mA$	$V_{CC} - 2.0$			V
$V_{OH}$	"H" output voltage P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>	$I_{OH} = -10mA$	$V_{CC} - 2.0$			V
$V_{OL}$	"L" output voltage P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>1</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub>	$I_{OL} = 10mA$			2.0	V
$V_{OL}$	"L" output voltage P6 <sub>0</sub>	$I_{OL} = 1.5mA$			0.5	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{INT_0} - \overline{INT_4}$ , $S_{IN1}$ , $S_{IN2}$ , $S_{CLK1}$ , $S_{CLK2}$ , $CNTR_0$ , $CNTR_1$	When using a non-port function		0.4		V
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$ , $X_{IN}$	$\overline{RESET} : V_{CC} = 2.8V$ to $5.5V$		0.5		V
$V_{T+} - V_{T-}$	Hysteresis $X_{CIN}$			0.5		V
$I_{IH}$	"H" input current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub> , PB <sub>0</sub> , PB <sub>1</sub>	$V_i = V_{CC}$			5.0	$\mu A$
$I_{IH}$	"H" input current P4 <sub>0</sub>	$V_i = V_{CC}$			5.0	$\mu A$
$I_{IH}$	"H" input current P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>3</sub> (Note 1)	$V_i = V_{CC}$			5.0	$\mu A$
$I_{IH}$	"H" input current $\overline{RESET}$ , $X_{CIN}$	$V_i = V_{CC}$			5.0	$\mu A$
$I_{IH}$	"H" input current $X_{IN}$	$V_i = V_{CC}$		4.0		$\mu A$
$I_{IL}$	"L" input current P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P4 <sub>1</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , PA <sub>0</sub> -PA <sub>7</sub> , PB <sub>0</sub> , PB <sub>1</sub>	$V_i = V_{SS}$			-5.0	$\mu A$
$I_{IL}$	"L" input current P4 <sub>0</sub>	$V_i = V_{SS}$			-5.0	$\mu A$
$I_{IL}$	"L" input current P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>3</sub> (Note 1)	$V_i = V_{SS}$			-5.0	$\mu A$
$I_{IL}$	"L" input current $\overline{RESET}$ , $X_{CIN}$	$V_i = V_{SS}$			-5.0	$\mu A$
$I_{IL}$	"L" input current $X_{IN}$	$V_i = V_{SS}$		-4.0		$\mu A$
$I_{LOAD}$	Output load current P0 <sub>0</sub> -P0 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>	$V_{EE} = V_{CC} - 36V$ , $V_{OL} = V_{CC}$ , With output transistors off	150	500	900	$\mu A$
$I_{LEAK}$	Output leakage current P0 <sub>0</sub> -P0 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub>	$V_{EE} = V_{CC} - 38V$ , $V_{OL} = V_{CC} - 38V$ , With output transistors off (Except for reset)			-10	$\mu A$
$V_{RAM}$	RAM hold voltage	When clock is stopped	2.0		5.5	V
$I_{CC}$	Power supply current	In high-speed operation mode $f(X_{IN}) = 6.3MHz$ $f(X_{CIN}) = 32kHz$ Output transistors off A-D converter operating		7.5	15	$\mu A$
		In high-speed operation mode $f(X_{IN}) = 6.3MHz$ (in WIT state) $f(X_{CIN}) = 32kHz$ Output transistors off A-D converter stopped		1.0		$\mu A$
		In low-speed operation mode $f(X_{IN}) =$ stopped, $f(X_{CIN}) = 32kHz$ Low-power dissipation mode set ( $CM_5 = 0$ ) Output transistors off		60	200	$\mu A$
		In low-speed operation mode $f(X_{IN}) =$ stopped $f(X_{CIN}) = 32kHz$ (in WIT state) Low-power dissipation mode set ( $CM_5 = 0$ ) Output transistors off		20	40	$\mu A$
		All oscillation stopped (in STP state)	$T_a = 25^\circ C$	0.1	1.0	$\mu A$
		Output transistors off	$T_a = 85^\circ C$		10	

Note 1. Except when reading ports P8 or ports P9<sub>0</sub>-P9<sub>3</sub>

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**A-D CONVERTER CHARACTERISTICS**

( $V_{CC}=4.0$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-10$  to  $85^{\circ}C$ , high-speed operation mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	$V_{CC}=V_{REF}=5.12V$		$\pm 1$	$\pm 2.5$	LSB
$T_{CONV}$	Conversion time		49		50	$t_C$ ( $\phi$ )
$V_{REF}$	Reference input voltage		2		$V_{CC}$	V
$I_{VREF}$	Reference input current	$V_{REF}=5V$	50	150	200	$\mu A$
$I_{IA}$	Analog port input current			0.5	5.0	$\mu A$
$R_{LADDER}$	Ladder resistor			35		$k\Omega$

**TIMING REQUIREMENTS**

( $V_{CC}=4.0$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-10$  to  $85^{\circ}C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(RESET)}$	Reset input "L" pulse width		2.0			$\mu s$
$t_C(X_{IN})$	Main clock input cycle time ( $X_{IN}$ input)		158			ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width		40			ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width		40			ns
$t_C(X_{CIN})$	Sub clock input cycle time ( $X_{CIN}$ input)		2.0			ms
$t_{WH}(X_{CIN})$	Sub clock input "H" pulse width		0.5			ms
$t_{WL}(X_{CIN})$	Sub clock input "L" pulse width		0.5			ms
$t_C(CNTR)$	$CNTR_0$ , $CNTR_1$ input cycle time		4.0			$\mu s$
$t_{WH}(CNTR)$	$CNTR_0$ , $CNTR_1$ input "H" pulse width		1.6			$\mu s$
$t_{WL}(CNTR)$	$CNTR_0$ , $CNTR_1$ input "L" pulse width		1.6			$\mu s$
$t_{WH}(INT)$	$INT_0$ - $INT_4$ input "H" pulse width		80			ns
$t_{WL}(INT)$	$INT_0$ - $INT_4$ input "L" pulse width		80			ns
$t_C(SCLK)$	Serial clock input cycle time		1.0			$\mu s$
$t_{WH}(SCLK)$	Serial clock input clock "H" pulse width		400			ns
$t_{WL}(SCLK)$	Serial clock input clock "L" pulse width		400			ns
$t_{SU}(SCLK-S_{IN})$	Serial input setup time		200			ns
$t_H(SCLK-S_{IN})$	Serial input hold time		200			ns

**SWITCHING CHARACTERISTICS**

( $V_{CC}=4.0$  to  $5.5V$ ,  $V_{SS}=0V$ ,  $T_a=-10$  to  $85^{\circ}C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH}(SCLK)$	Serial clock output "H" pulse width	$C_L=100pF$ , $R_L=1k\Omega$	$t_C/2-160$			ns
$t_{WL}(SCLK)$	Serial clock output "L" pulse width	$C_L=100pF$ , $R_L=1k\Omega$	$t_C/2-160$			ns
$t_d(SCLK-S_{OUT})$	Serial output delay time				$0.2t_C$	ns
$t_v(SCLK-S_{OUT})$	Serial output hold time		0			ns
$t_f(SCLK)$	Serial clock output fall time	$C_L=100pF$ , $R_L=1k\Omega$			40	ns
$t_r(Pch-strg)$	P-channel high-breakdown voltage output rise time (Note 1)	$C_L=100pF$ , $V_{EE}=V_{CC}-36V$		55		ns
$t_r(Pch-weak)$	P-channel high-breakdown voltage output rise time (Note 2)	$C_L=100pF$ , $V_{EE}=V_{CC}-36V$		1.8		$\mu s$

Note 1. When bit 0 of the high-breakdown voltage port control register (address 0038<sub>16</sub>) is at "0"

2. When bit 0 of the high-breakdown voltage port control register (address 0038<sub>16</sub>) is at "1"

**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

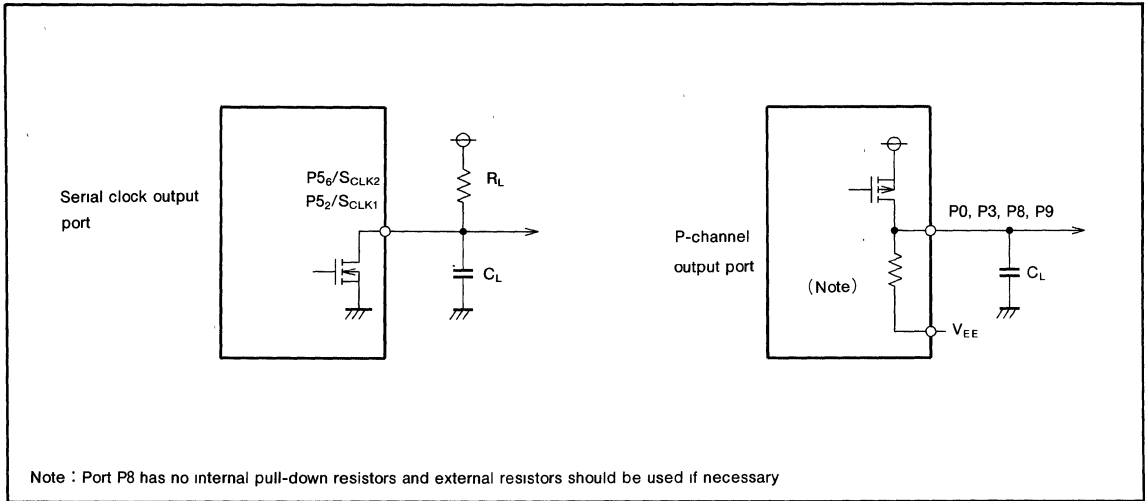


Fig. 43 Output switching characteristics measurement circuit



**SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER**

**Timing Chart**

